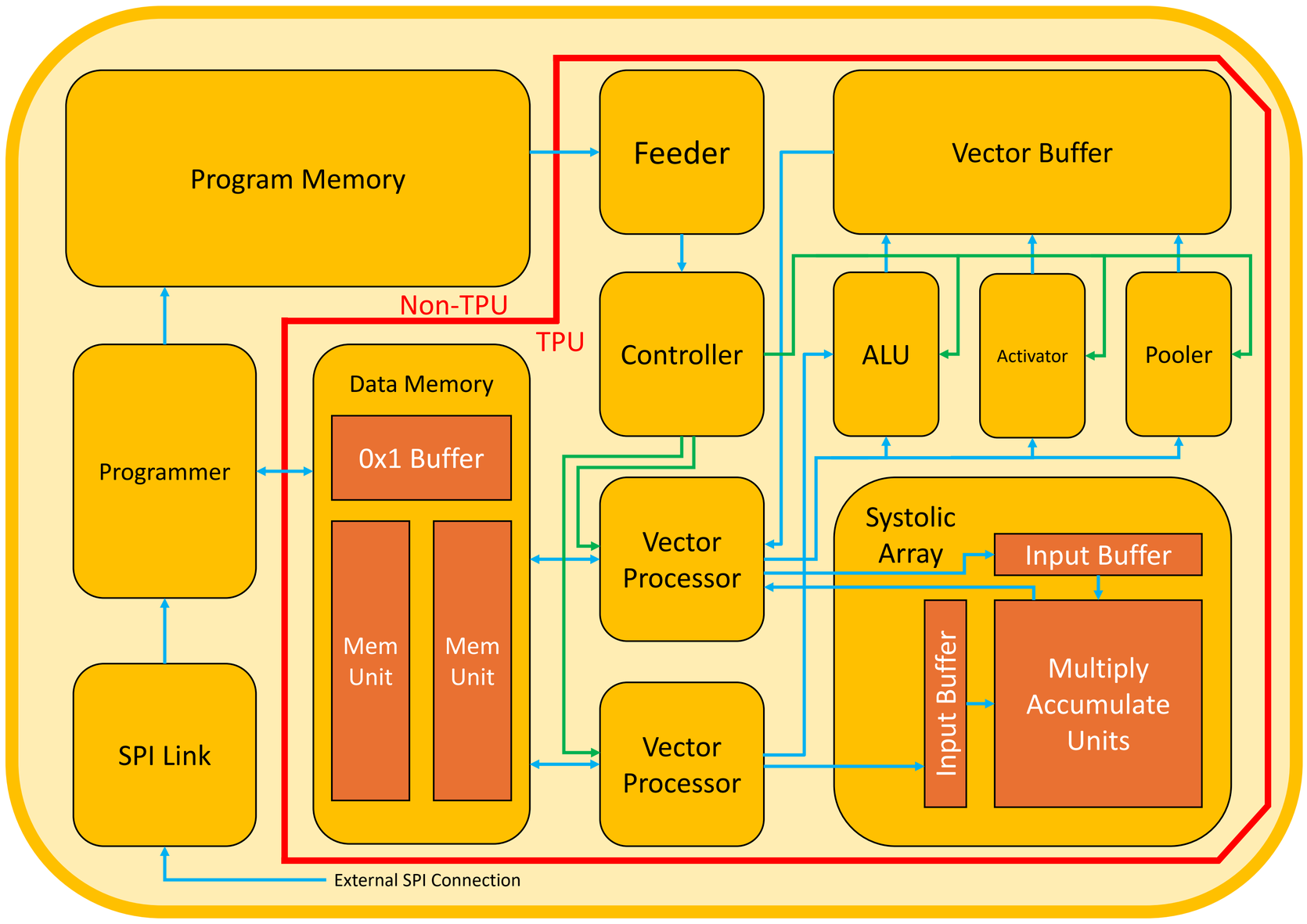
Functional TPU: A Proof-of-Concept AI Accelerator

Gabe Litteken,
Peter Jamieson
Department of Electrical and Computer Engineering, Miami University

Functional TPU (Tensor Processing Unit) is a processor (in Verilog) that runs small neural networks using hardware acceleration to speed up computation. Our *Functional TPU* illustrates a possible architecture that students and researchers can freely explore and reuse to create their own TPUs.

The Heart of a TPU: The Systolic Array

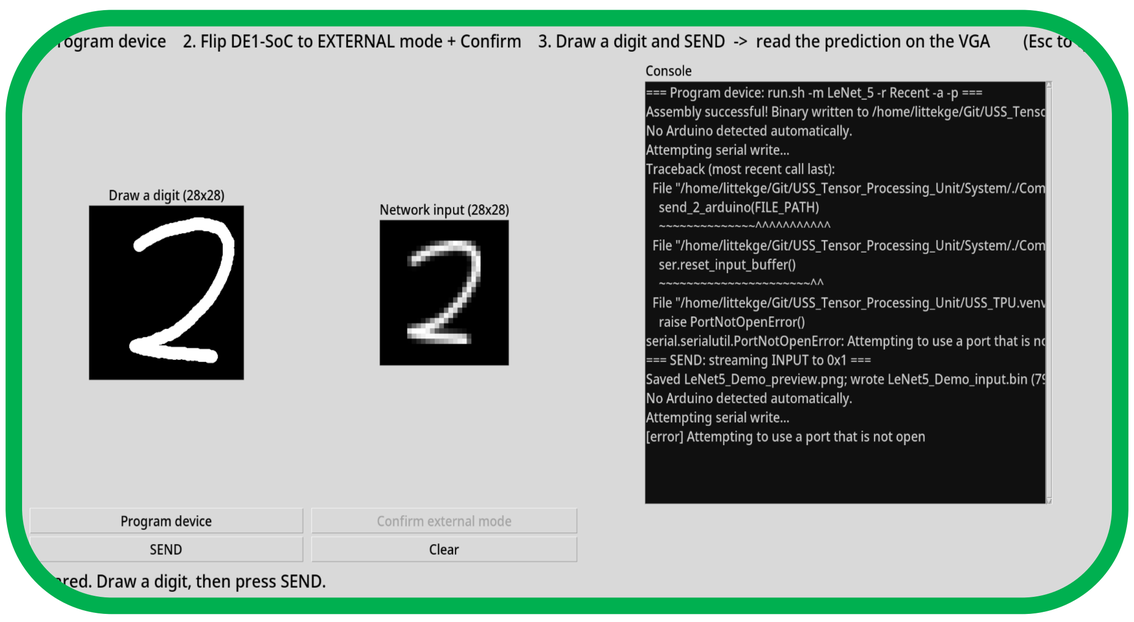
The primary method of hardware acceleration in the *Functional TPU* is the *systolic array.* A systolic array is composed of many *multiply-accumulate units* linked together to maximize reuse of data during matrix multiplications.

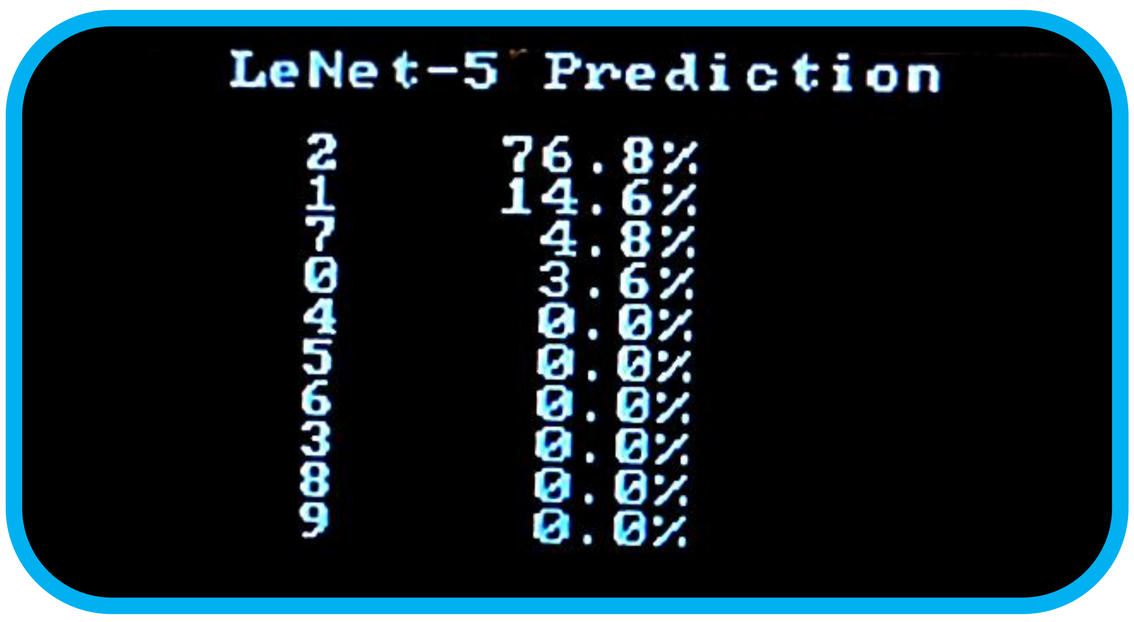


TPU Diagram

Control Signal — Data Signal

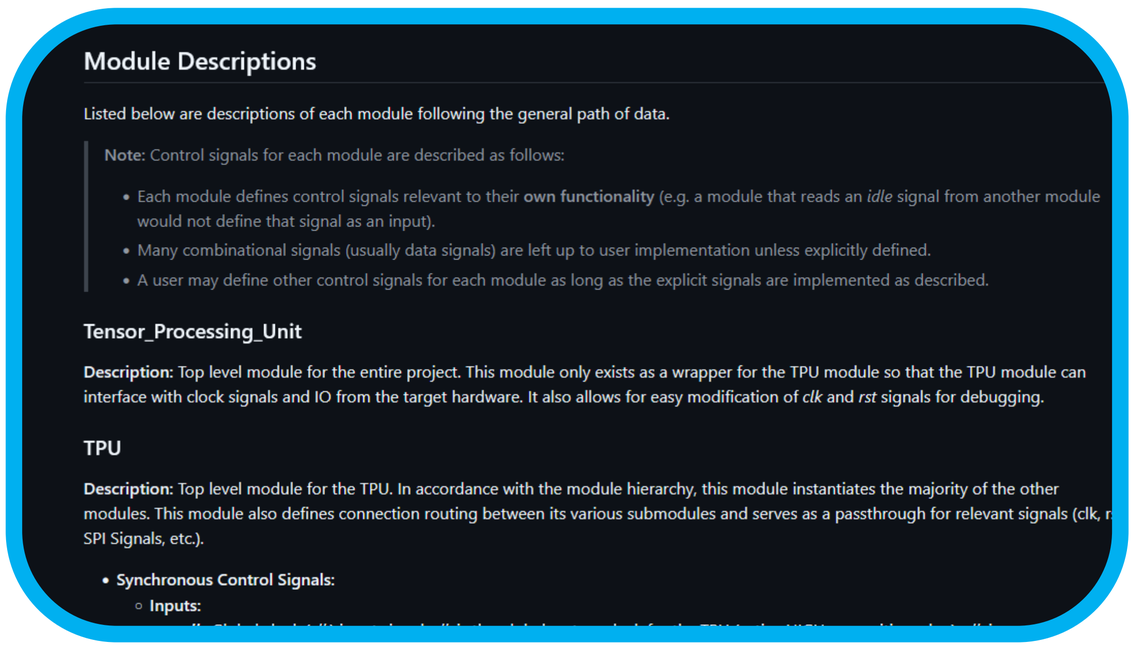
Digit Recognition!





The Dark Factory Approach

The Dark Factory development approach (using AI to write code) made a functional TPU possible. The TPU's layout and functions were planned and documented in multiple spec documents, then converted to Verilog HDL using Claude Code. The design was implemented on an FPGA.



Access Design At:

https://github.com/littekge/USS_Tensor_Processing_Unit