Odin II - An Open-source Verilog HDL Synthesis Tool for CAD Research

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**Miami U.*

†UNB

‡Simon Fraser

For sale!

Verilog HDL Synthesis Tool !!!

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ODIN
DM-53-98

INTERNATIONAL CAR CO.


ODIN


ODIN II*
DM-53-98

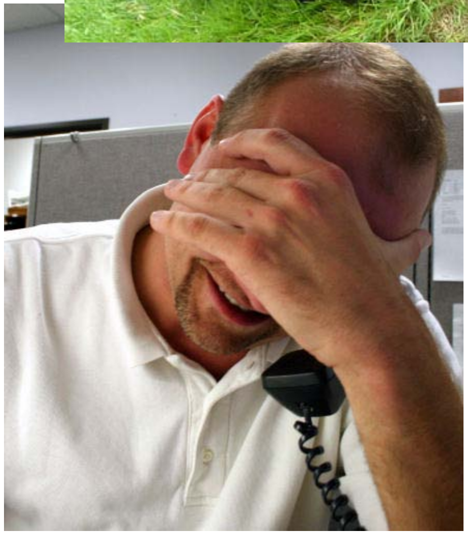
IMPORTANT INFORMATION

Annual Percentage Rate (APR) for Purchases	0% until the last day of the billing period ending during May 2010*; then the standard APR, 10.99% variable
Other APRs	**Balance Transfers:** 0% until the last day of the billing period ending during May 2010*; then the standard APR for purchases **Cash Advances:** 23.99% variable **Default Rates:** Up to 30.99%* fixed for billing periods ending on or before May 1, 2009; up to 29.99%* variable for billing [illegible] ending after May 1, 2009.
Variable Rate Information	The standard purchase APR may vary monthly and equals the Prime Rate + 7.74%. The cash advance APR may [illegible] and equals the Prime Rate + 20.74%. For billing periods ending after May 1, 2009, the default APR may vary [illegible] Prime Rate plus up to 27.99%, but such rate will never exceed 29.99%.†
Grace Period for Repayment of the Balance of Purchases	At least 25 days when you pay your balance in full each month
Method of Computing the Balance for Purchases	Average Daily Balance (including new purchases)
Foreign Currency Transaction Fee	None for billing periods ending on or before May 1, 2009; 2% of the U.S. dollar amount of [illegible] foreign currency for billing periods ending after May 1, 2009.
Annual Fee: NONE	**Minimum Finance Charge:** $0.50

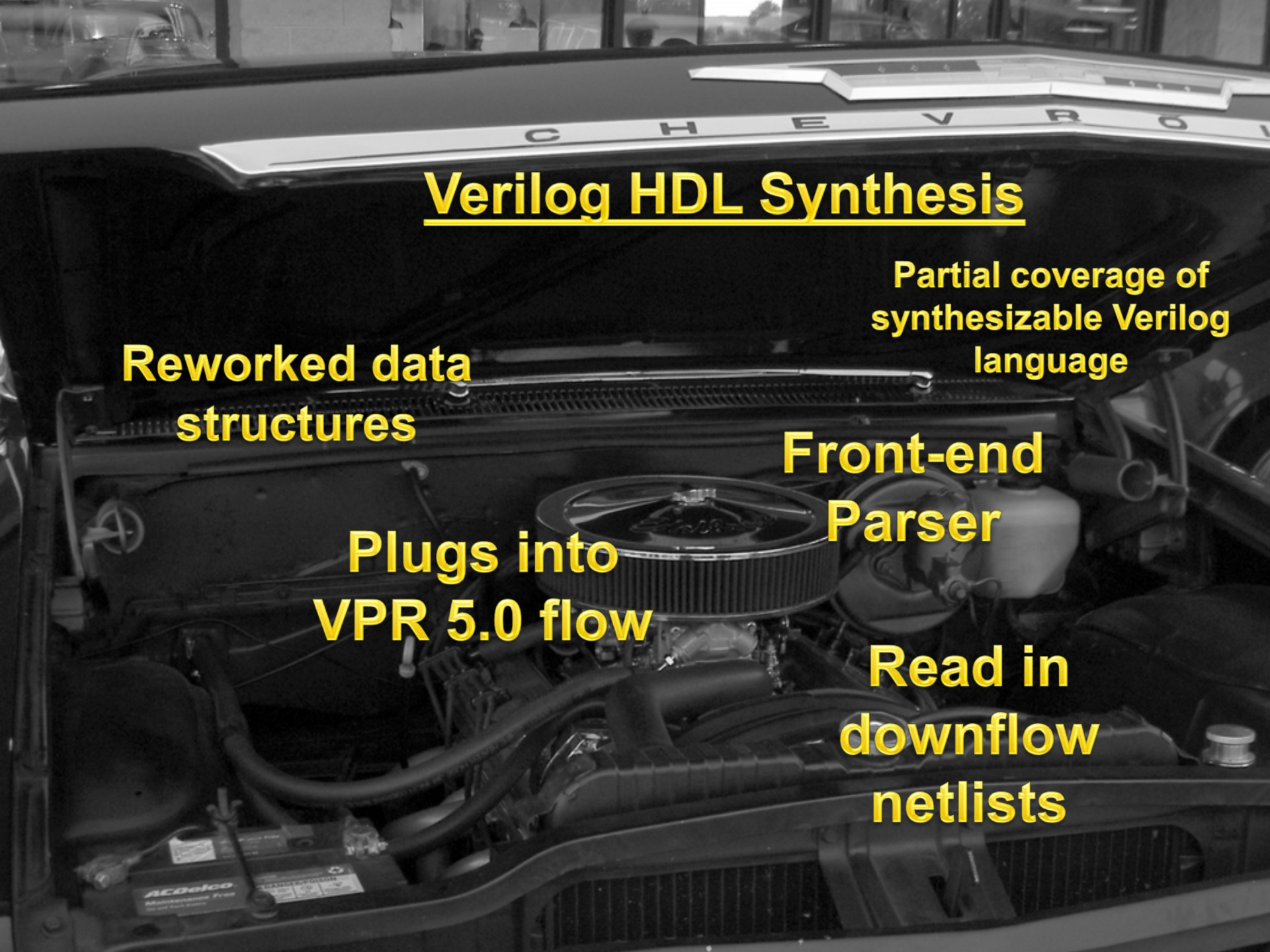
BALANCE TRANSFER TRANSACTION FEE: 3% for each balance transfer made under this offer. **CASH ADVANCE TRANSACT**[illegible]: 3% for each cash advance, with a minimum of $5 and no maximum. **LATE FEE:** $19 on balances up to $250 and $39 on balances over $250. **OVERLIMIT FEE:** $1[illegible] balances up to $500, and $39 on balances over $500.

*DEFAULT RATE: If you are late making a payment or your account is overlimit twice, any introductory/special rates will end and we may incr[illegible] your APRs to a Default Rate. Your Default Rate is determined based on factors such as your current APRs, your payment history with us and your general credit history. See Cardmember Agreement for details.

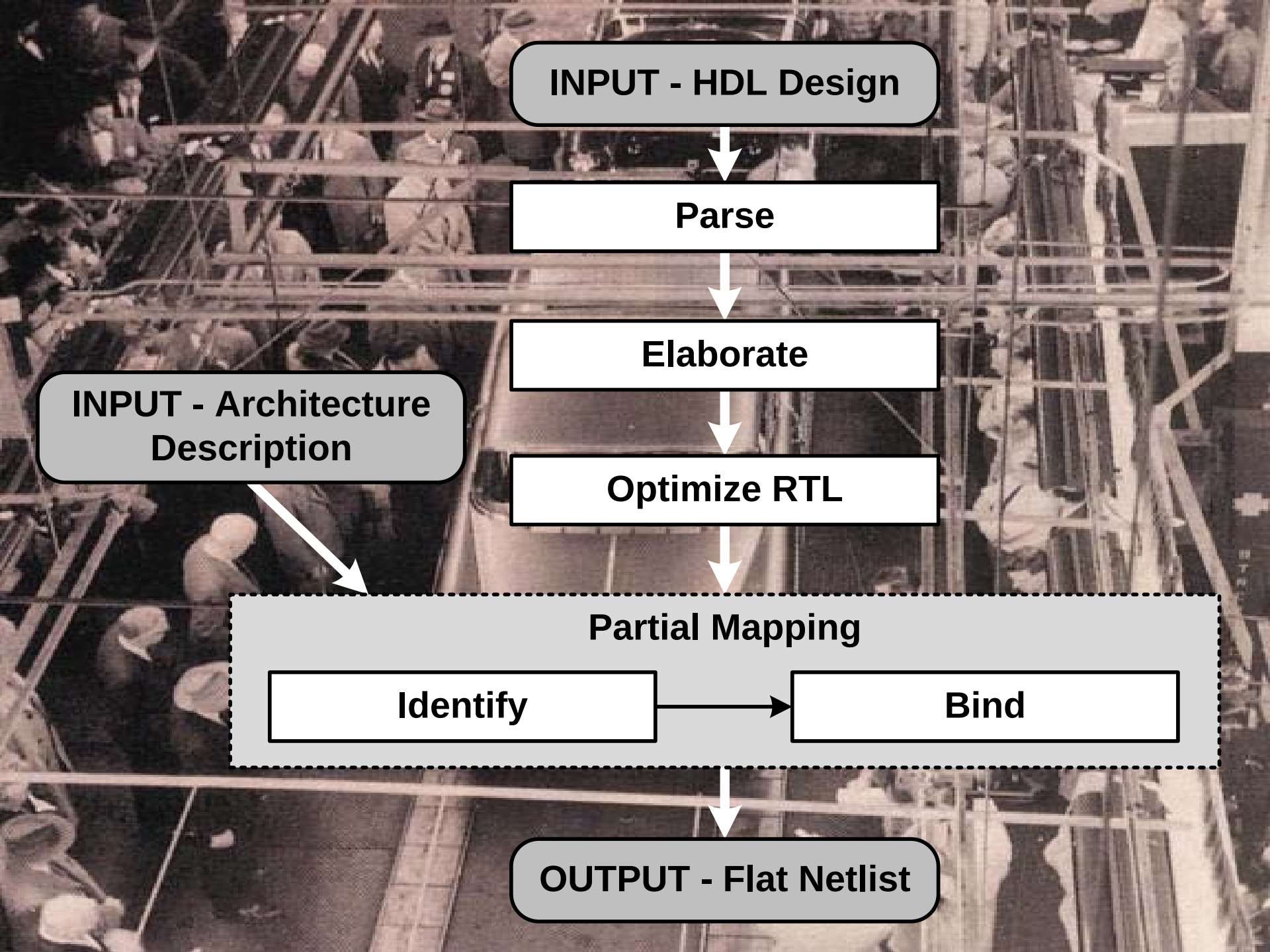
†The Prime Rate used is the highest prime rate listed in *The Wall Street Journal* on the last business day of the month.

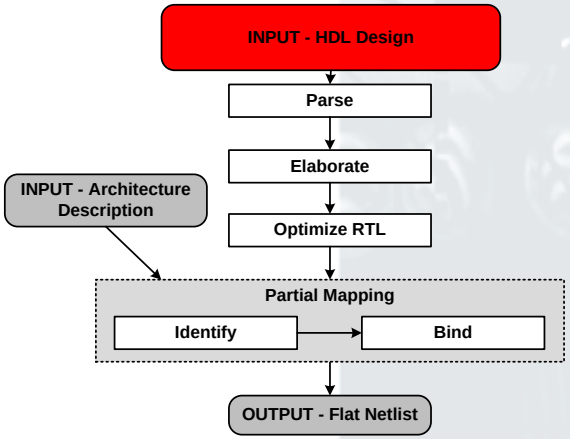



ODIN II


Verilog HDL Synthesis
Partial coverage of synthesizable Verilog language
Reworked data structures
Front-end Parser
Plugs into VPR 5.0 flow
Read in downflow netlists

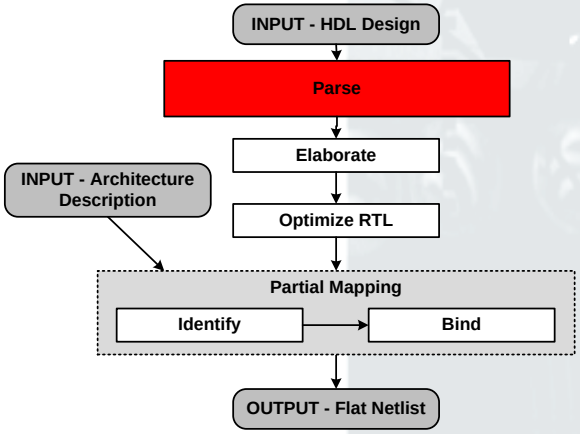

Academic Open-source

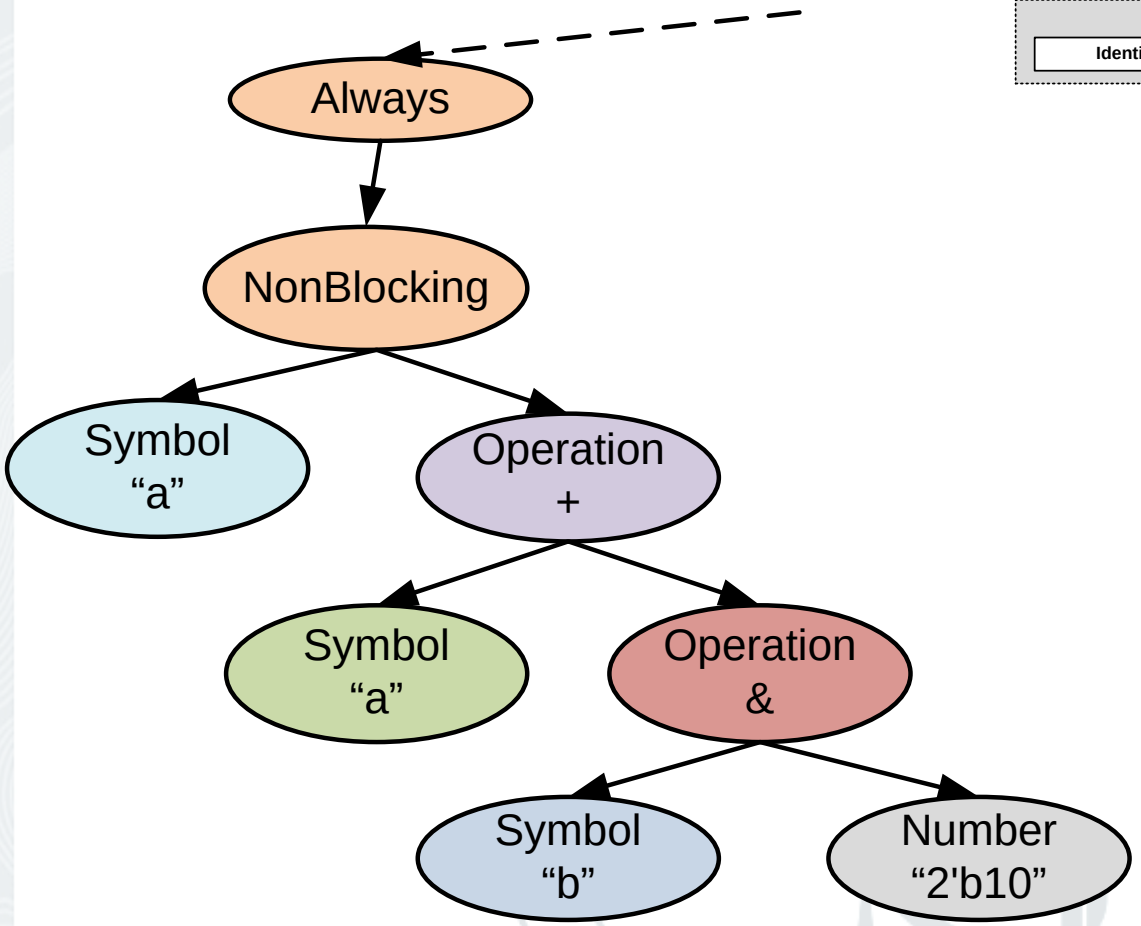

INPUT - HDL Design
Parse
Elaborate
INPUT - Architecture Description
Optimize RTL
Partial Mapping
Identify
Bind
OUTPUT - Flat Netlist




```
always @(posedge clk)
begin
        a <= a + b & 2'b10;
end
```

```
always @(posedge clk)
begin
        a <= a + b & 2'b10;
end
```





ABSTRACT SYNTAX TREE (AST)

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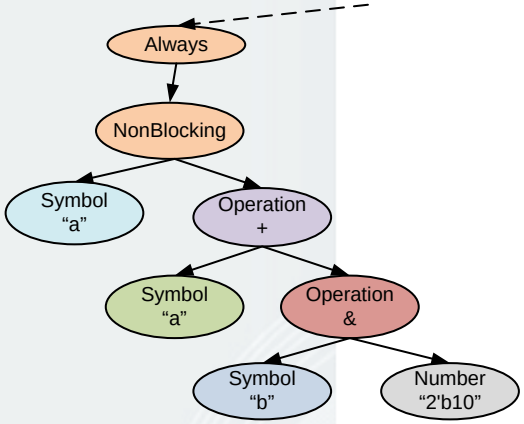

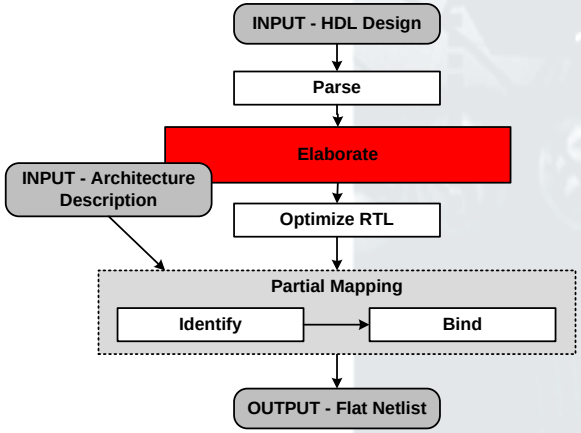

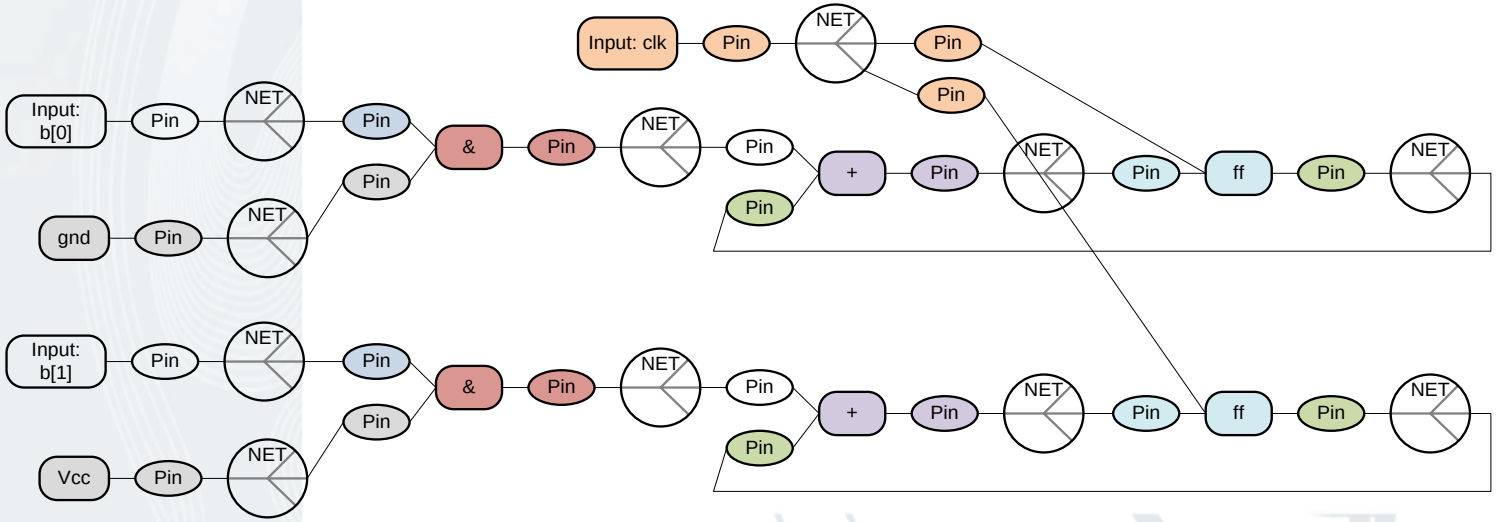

FLATTENED NETLIST

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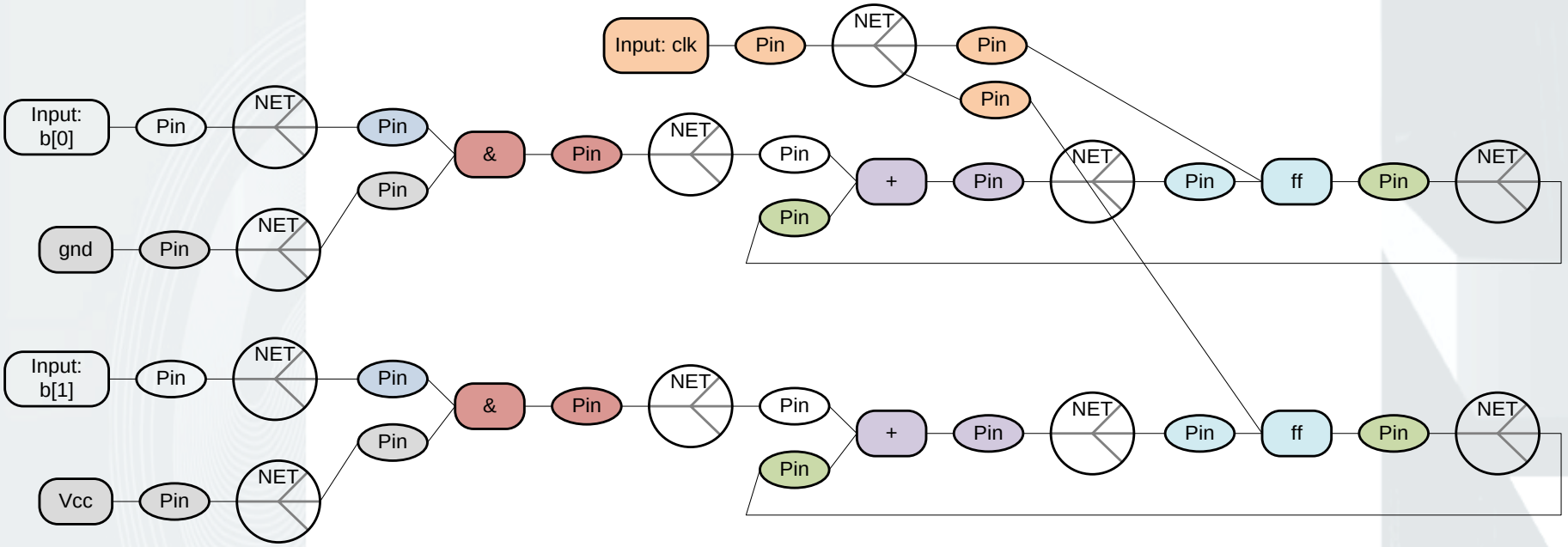
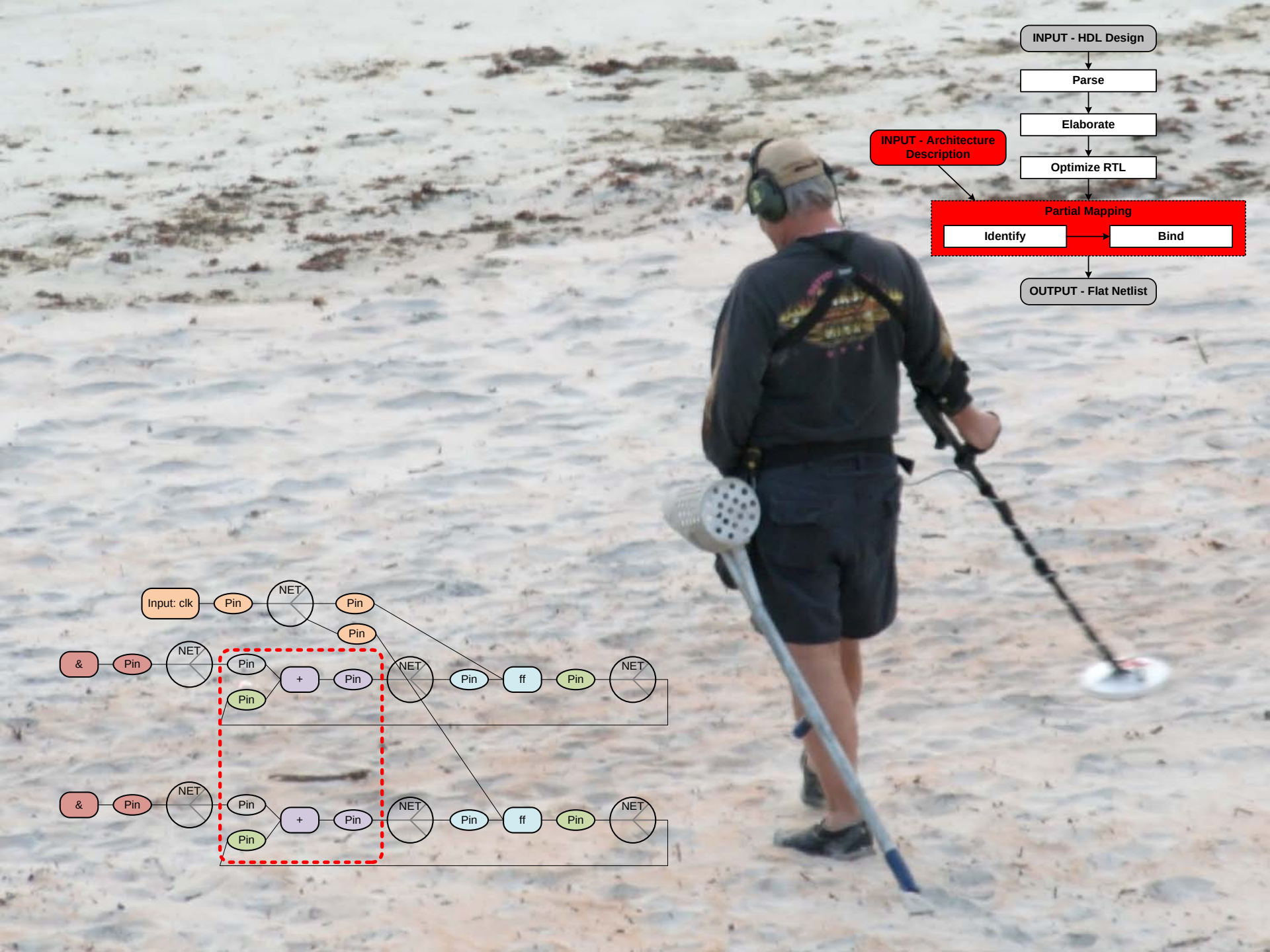
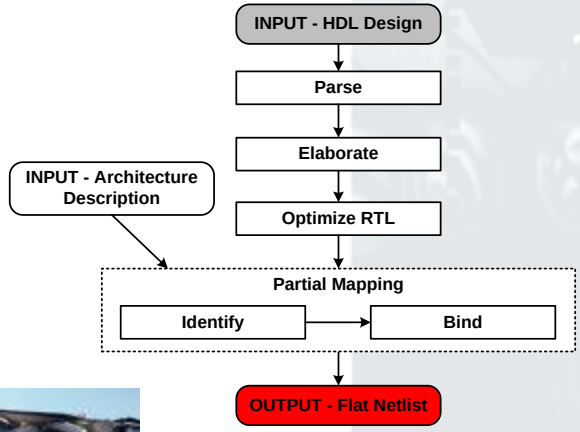



INPUT - HDL Design
Parse
Elaborate
INPUT - Architecture Description
Optimize RTL
Partial Mapping
Identify
Bind
OUTPUT - Flat Netlist
POTENZA
BRIDGESTONE
BBS
BBS
BBS


INPUT - HDL Design
Parse
Elaborate
INPUT - Architecture Description
Optimize RTL
Partial Mapping
Identify
Bind
OUTPUT - Flat Netlist
Input: clk
Pin
NET
&
+
ff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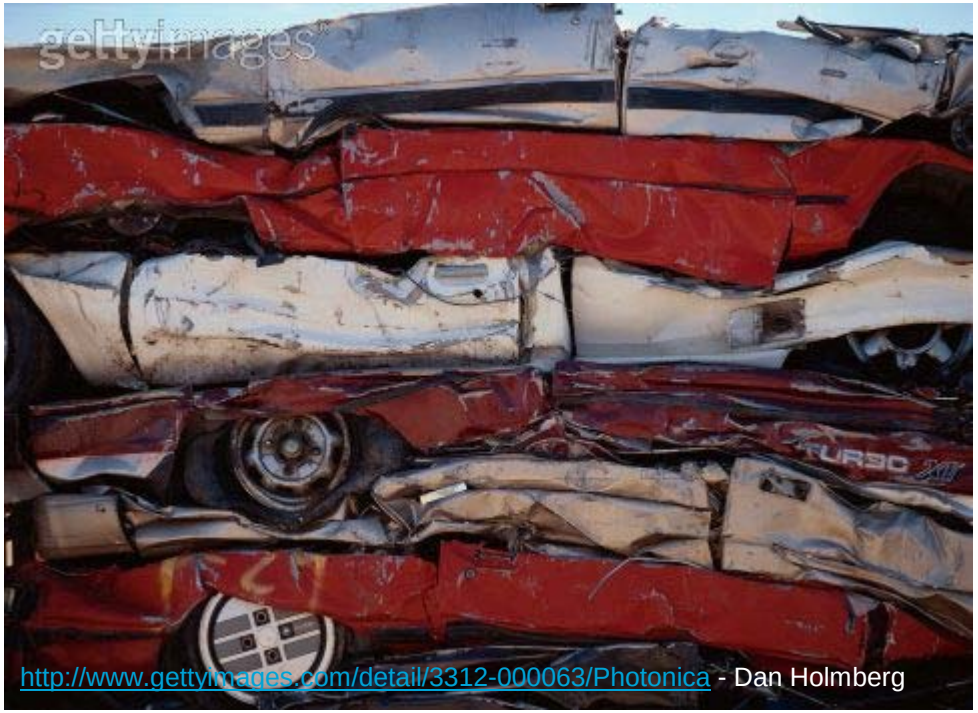
gettyimages
http://www.gettyimages.com/detail/3312-000063/Photonica - Dan Holmberg


AutoScan


COLOR POWER GRAPHIC
OPTN
VARS
MENU
EXIT
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sin
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AC/ON
EXP
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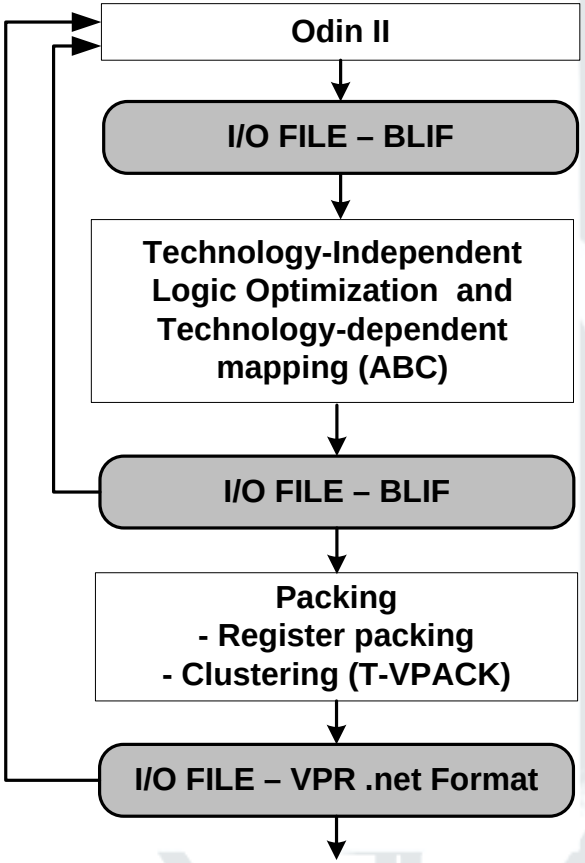

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