

# Benchmarking Reconfigurable Architectures in the Mobile Domain

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Peter Jamieson, Tobias Becker, Wayne Luk, Peter Y. K. Cheung, Tero Rissa, Teemu Pitkanen

# Motivating FPGAs in mobile domain

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- The good:
  - Performance
  - Flexibility
    - Logistics
    - Standards
    - Pin expansion
- The bad:
  - Silicon Area (\$)
  - Power consumption

# Energy problem

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- Power's the problem, but there's a huge market

Where is the research?

# Need an idea of where to look

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- Motivate and evaluate the problem with...

## BENCHMARKS



# Existing benchmarks: Challenges

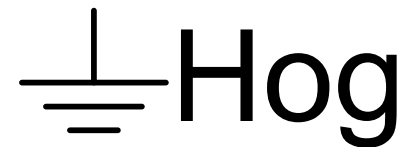
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- Hard to compare different architectures
  - DSP Processors vs. FPGA
- May not include input stimuli (intermittent)
- Don't specifically target mobile applications

# GroundHog 2009

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- Benchmark suite for reconfigurable architectures targeting the mobile domain

The logo for GroundHog, featuring a stylized groundhog icon (a vertical line with a horizontal line and two parallel lines below it) followed by the word "Hog" in a bold, sans-serif font.

# Fundamental goals

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- Mobile vendors
  - evaluate reconfigurable architectures
- Researchers
  - help drive low power device research

# Basic details of GroundHog 2009

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1. Fabric Analysis
  - evaluate fine-grain FPGA logic fabric energy consumption
2. 6 designs
  - applications in mobile domain
3. Tools to help build test benches and verification



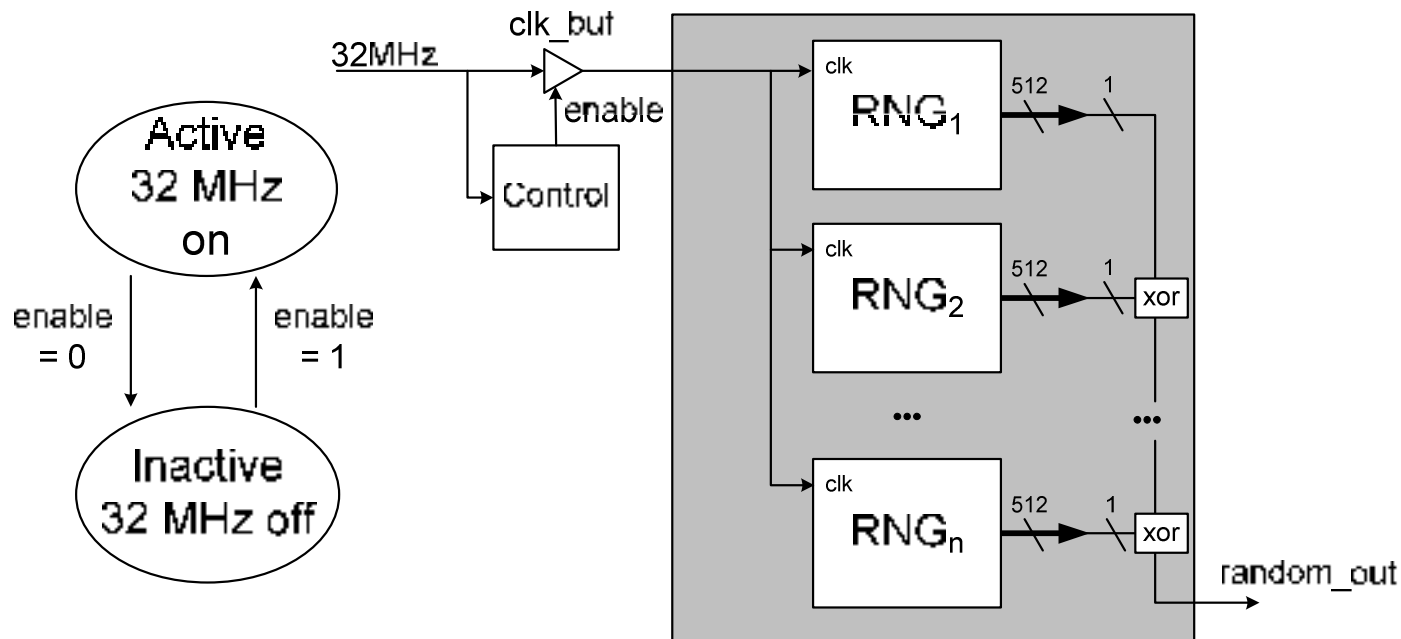
# 1. Fabric analysis

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- Fine-grain FPGA logic fabric power analysis
  - Stress test of logic fabric (logic + wires)
  - Quick analysis
  - Indicator of current state of the art

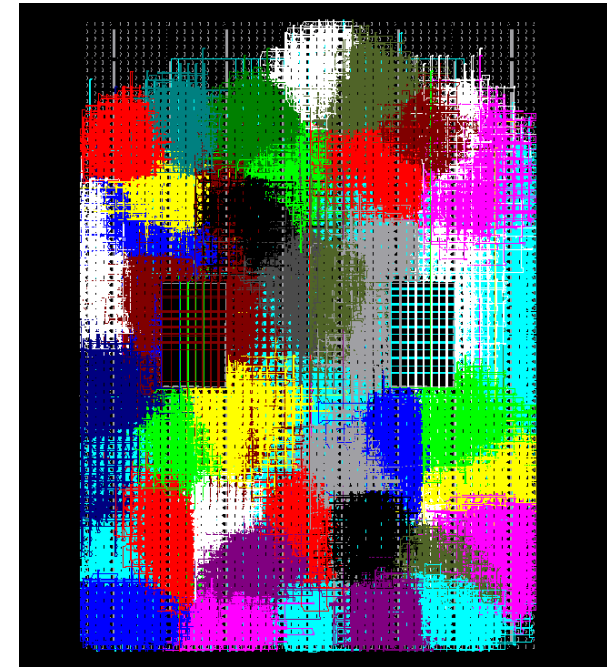
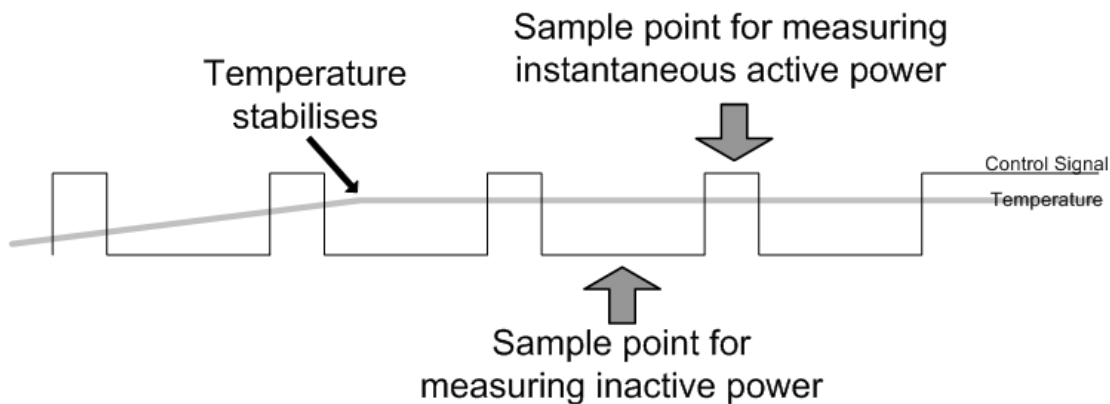
# How?

- Use random number generation cores as worst case for device activity [D.Thomas]



# Basic idea

- Fill the FPGA with RNGs – 60%
- Clock X MHz, duty cycle 1%-100%
  - measure power and temperature over duty cycle



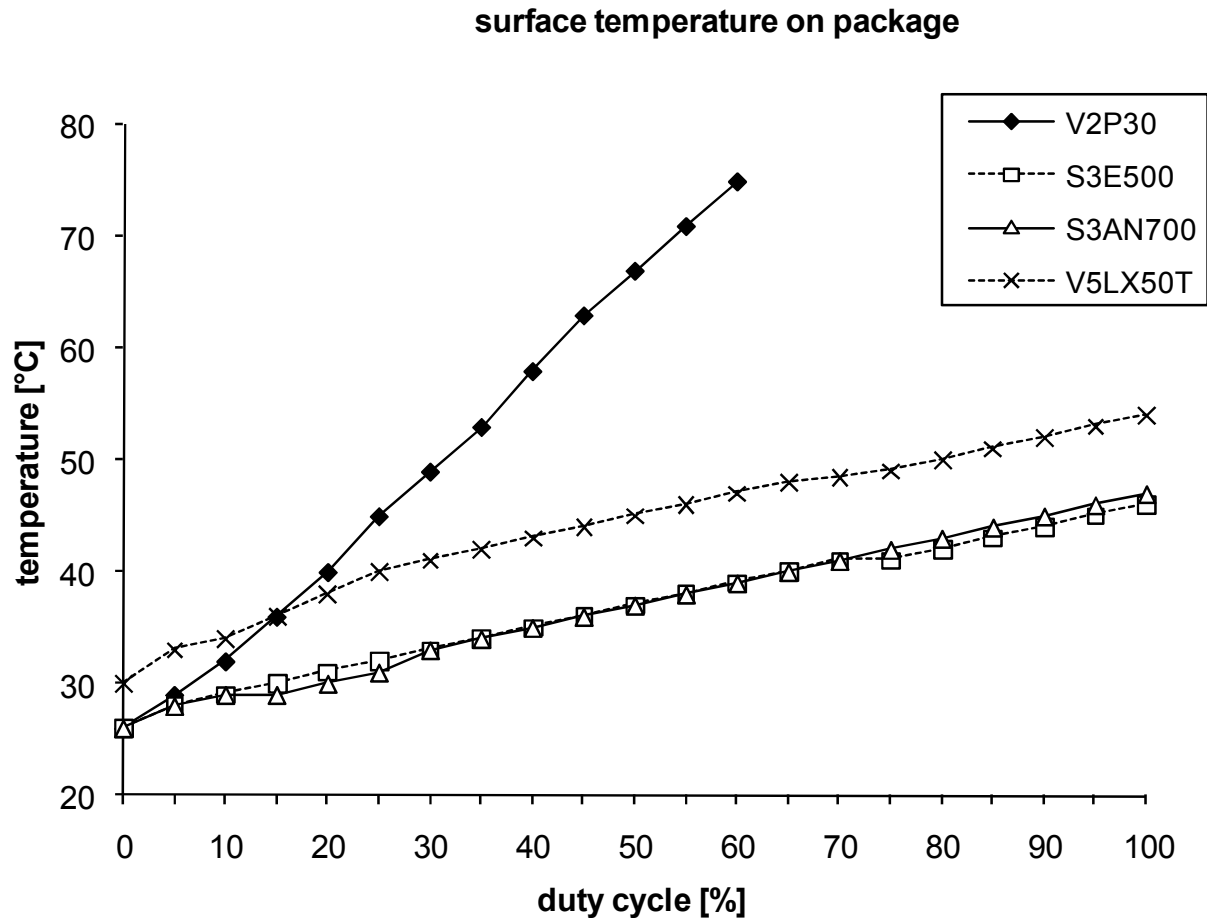
- Xilinx Virtex-II Pro 30
  - 48 RNGs, ~90% logic utilisation

# Measured FPGAs



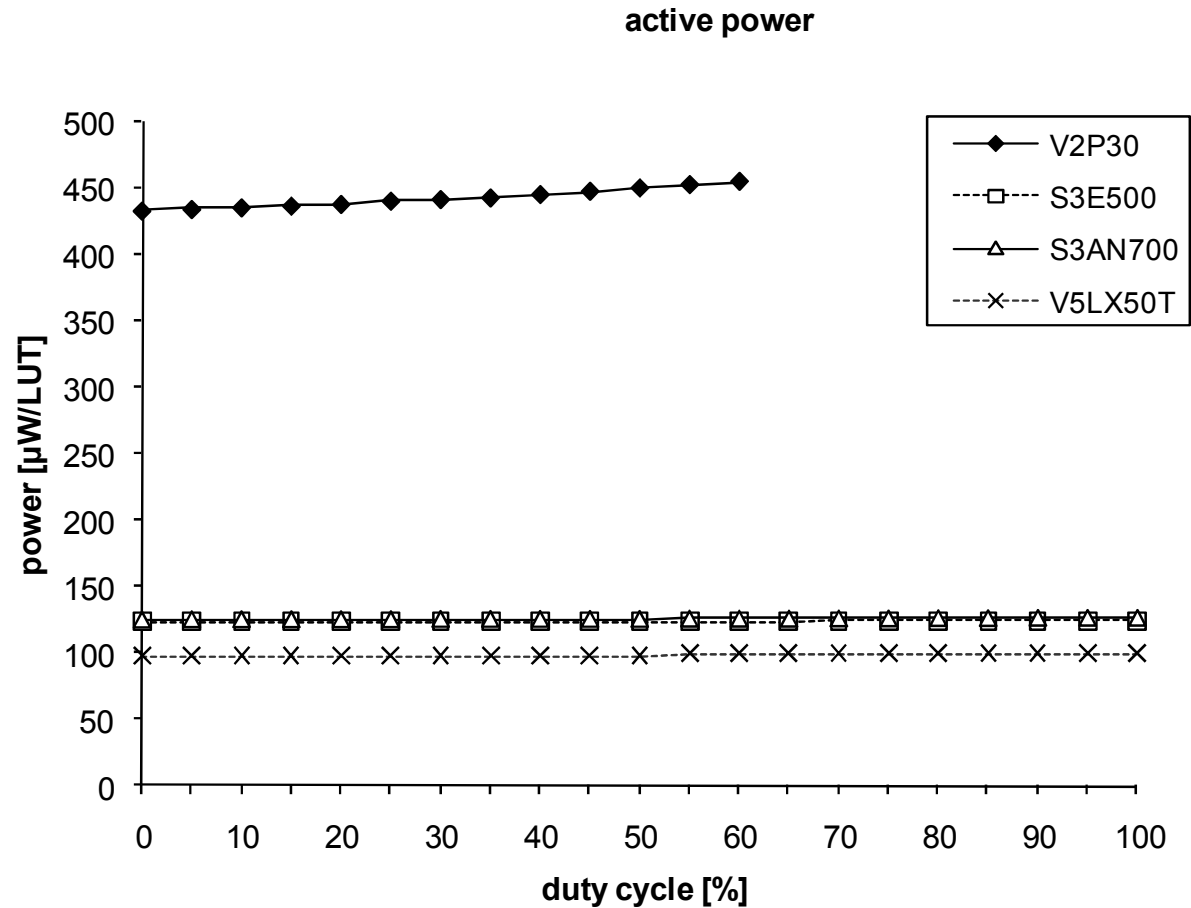
FPGA	Process Technology	Number of RNGs	Logic Utilisation
Virtex-II Pro	130nm	48	89.7%
Spartan-3E	90nm	16	88%
Spartan-3AN	90nm	21	91.3%
Virtex-5	65nm	50	88.8%

# Temperature of FPGAs



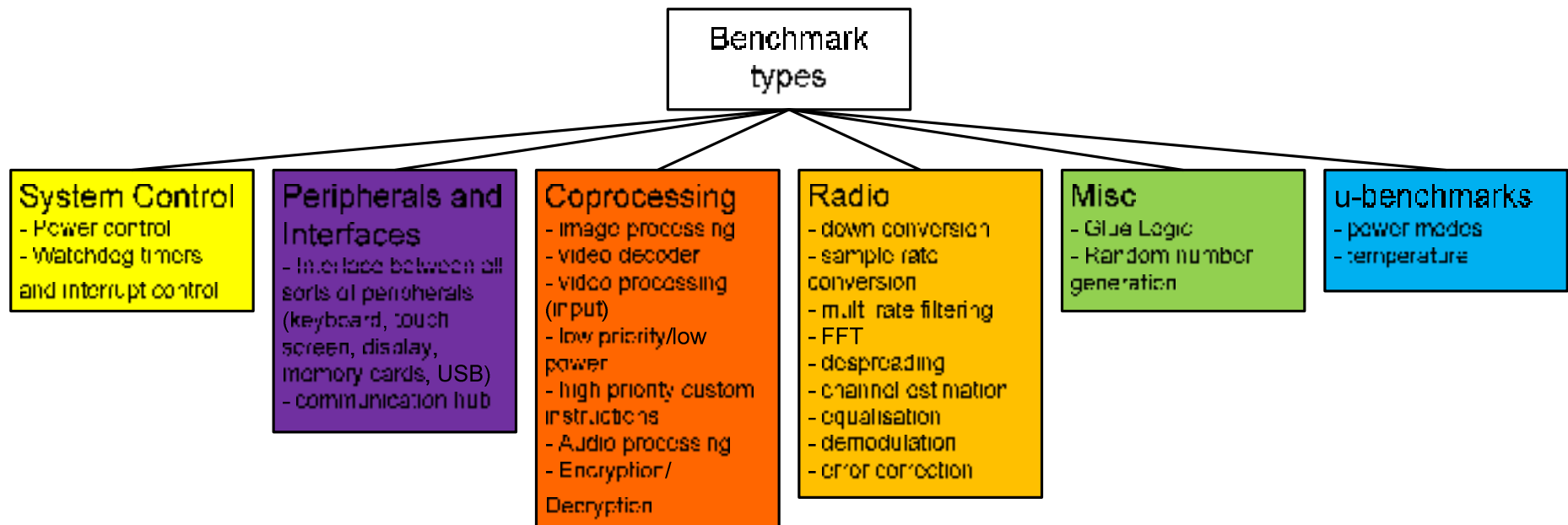
- 100MHz clocks

# Active power of FPGAs

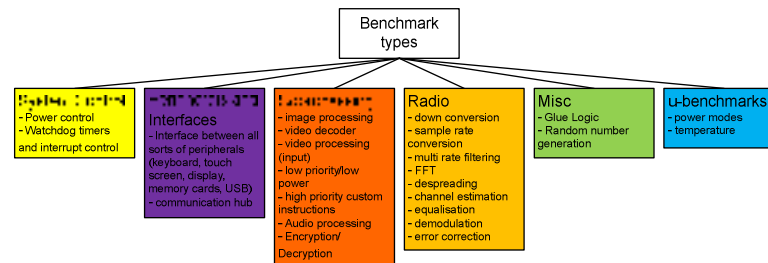


## 2. Six designs - possible benchmarks

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# Six current designs

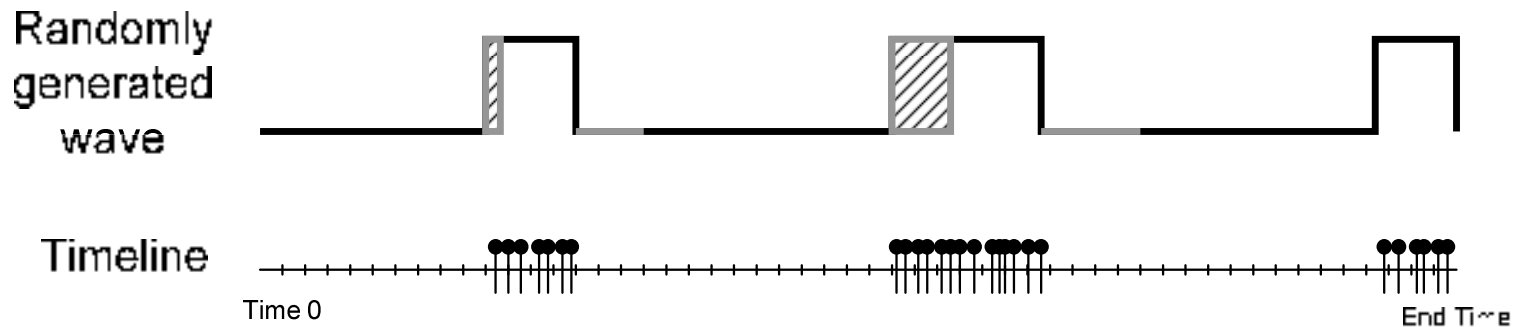


- GH09.B.1 - Port Expander and Keypad Controller
- GH09.B.2 - Glue Logic
- GH09.B.3 - Cryptography
- GH09.B.4 - Data Compression
- GH09.B.5 - Bridge Chip
- GH09.B.6 - 2D convolution

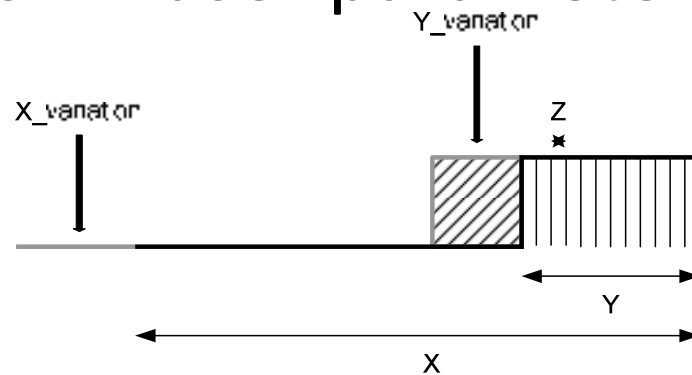


# 3. Tool for synthetic generation of Input Stimuli

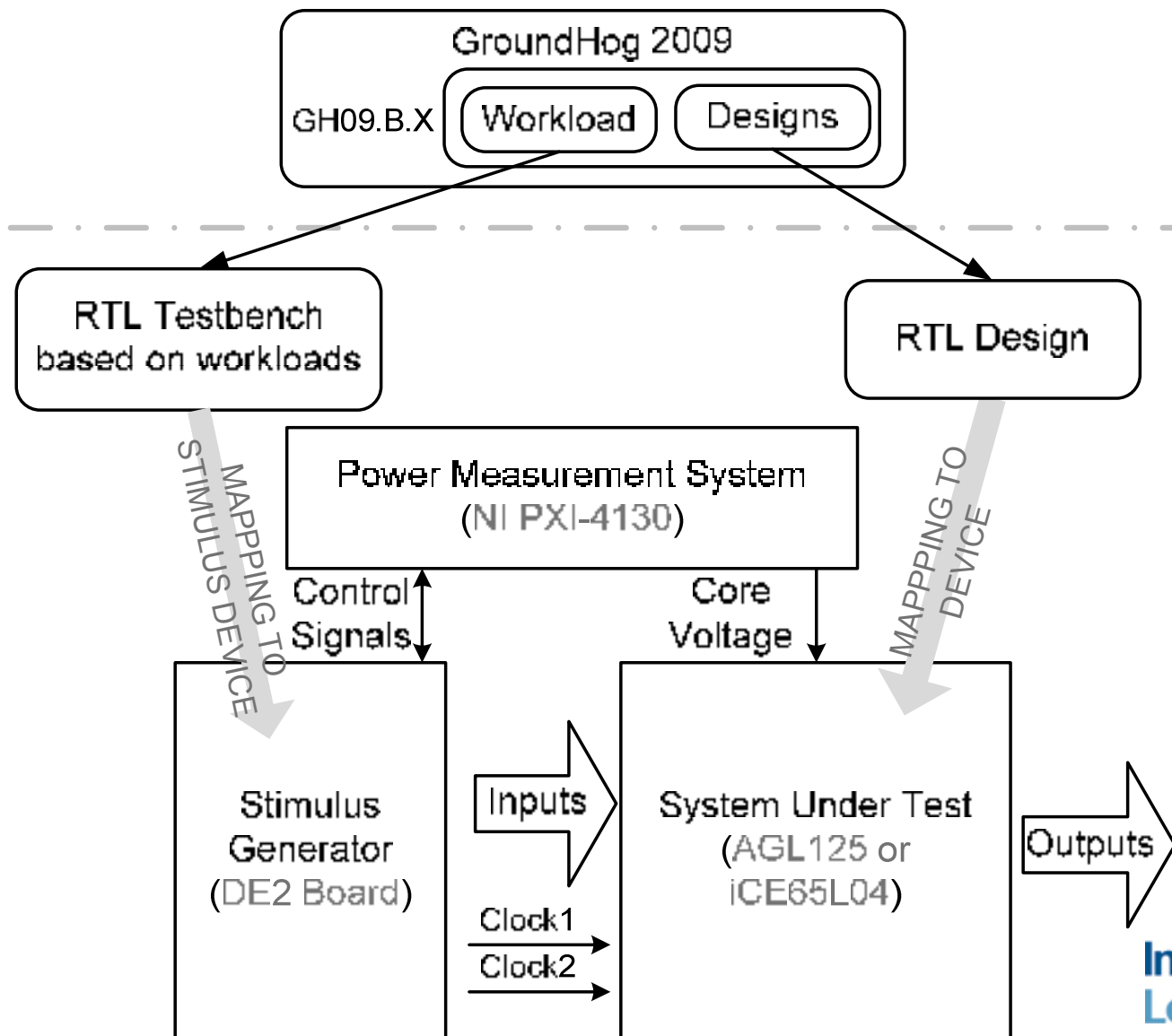
- Workload - Timeline of input stimuli
  - Per benchmark modelling of events



- software tool -> user parameters

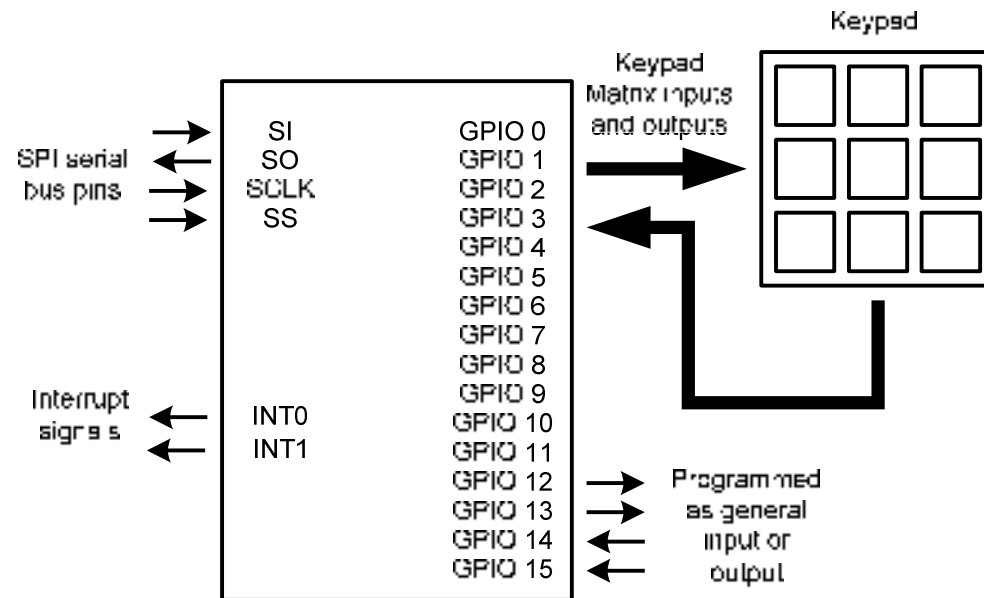


# Actual use of this benchmark



# Measuring GH09.B.1

- Port Expander and Keyboard controller
  - General purpose I/Os



# GH09.B.1 as 7x8 keypad

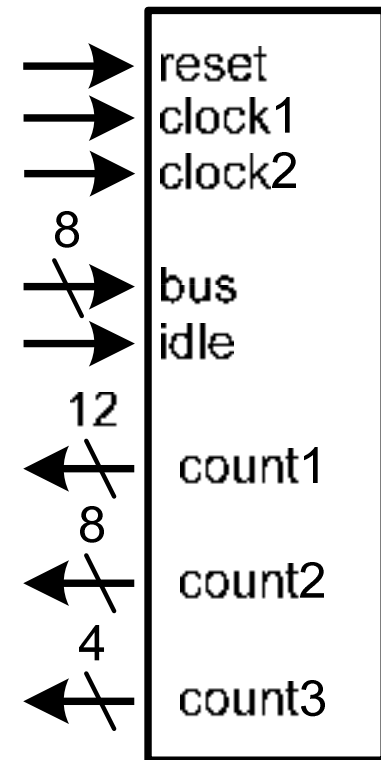


FPGA	Logic Utilisation	Operating Frequency	V <sub>cc</sub> (V)	I <sub>avg</sub> (mA)	P <sub>avg</sub> (mW)
AGL600	10%	32 MHz	1.5	3.751	5.628
AGL600	10%	32 MHz	1.2	2.951	3.541
AGL600	10%	150 KHz	1.5	0.091	0.137
AGL600	10%	150 KHz	1.2	0.059	0.071

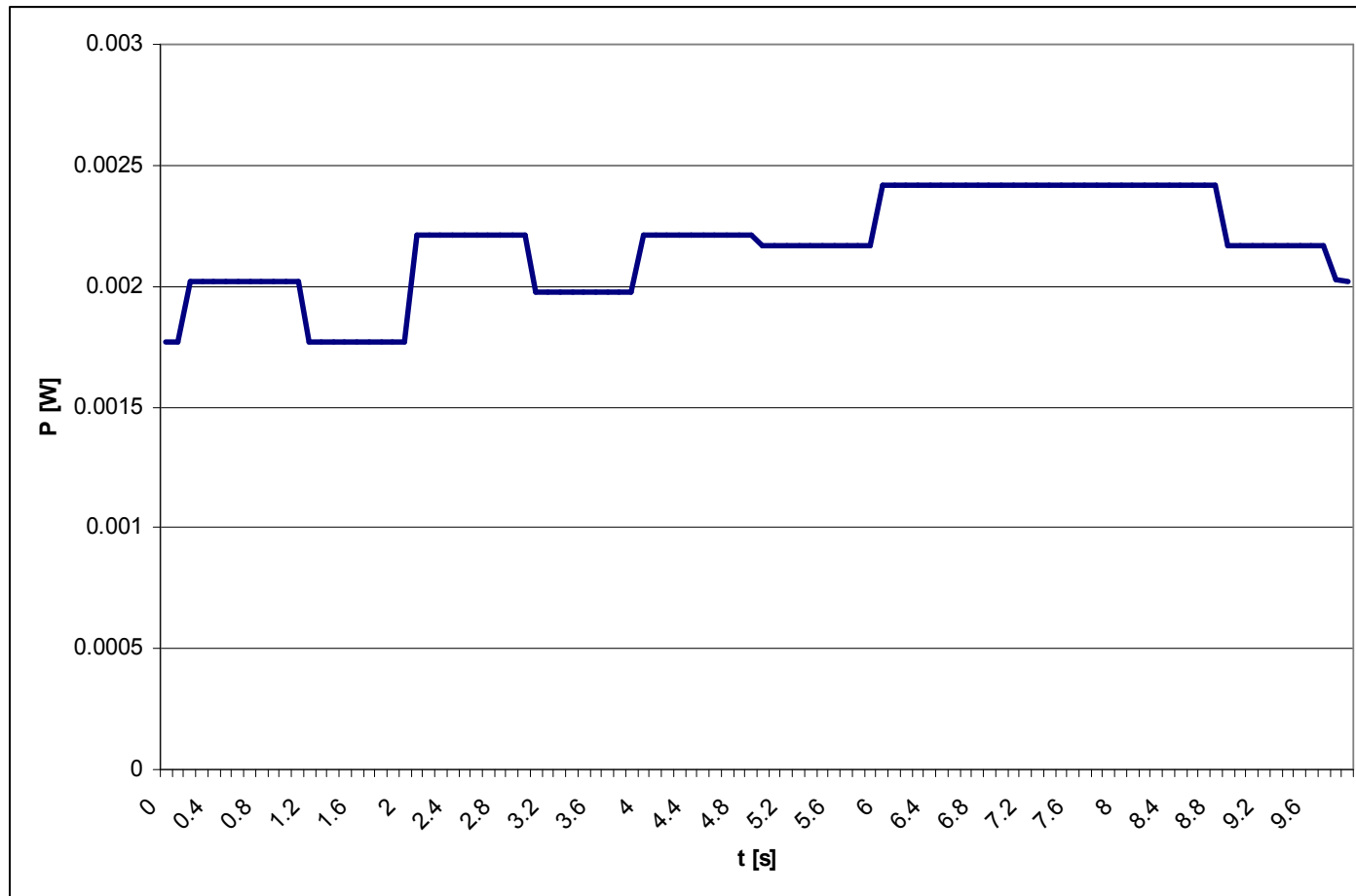
- Synthetically generated input (Z=25ms, Y=500ms, X=1000ms) and total time is 5 minutes

# Measuring GH09.B.2

- GH09.B.2 - Glue Logic
  - State Machine controls 3 adders
  - State Machine controlled by bus
  - Adders are each clocked by one of
    - No clock (idle)
    - Slow clock (150 KHz)
    - Fast clock (35 MHz)



# GH09.B.2 measurements over 10s



- Actel FPGA (AGL125), 1.2 V, 35 MHz

# GH09.B.2 over 5 minutes



FPGA	Logic Utilisation	Operating Frequency	$V_{cc}$ (V)	$I_{avg}$ (mA)	$P_{avg}$ (mW)
iCE65L04	4%	32 MHz	1.2	1.46	1.75

- Synthetically generated input (Z=1ms, Y=10ms, X=1000ms) and total time of 5 minutes

# Conclusion

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- Join the fun!
  - Download the suite including tools
    - <http://cc.doc.ic.ac.uk/projects/GROUNDHOG/>
  - Repository for communities designs
    - [http://www.opencores.org/?do=project&who=groundhog2009\\_repository](http://www.opencores.org/?do=project&who=groundhog2009_repository)
- Measured a range of devices

