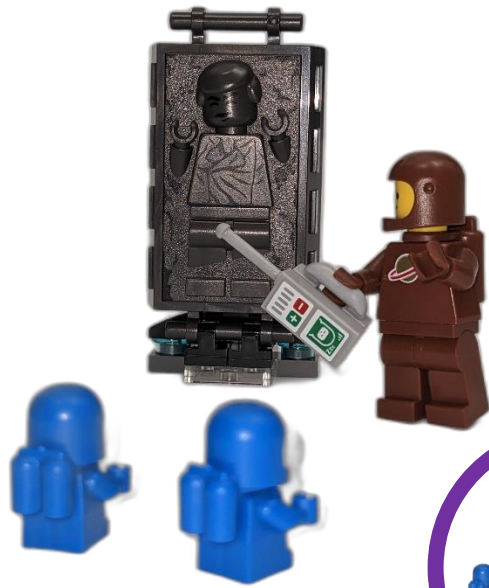


Case-based Learning Approach to Teach Students How to Read Academic Papers

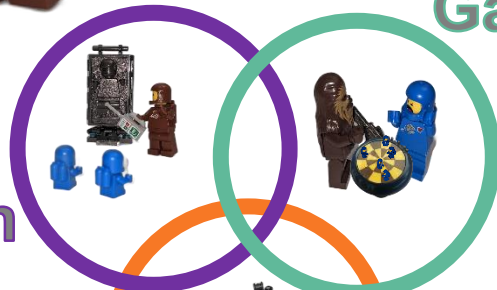
Peter Jamieson
Miami University



About Me



Education



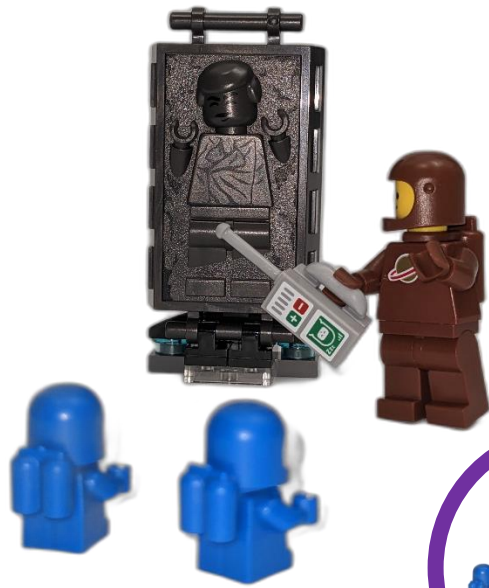
Games



Computer Engineering



About Me



Education



Games

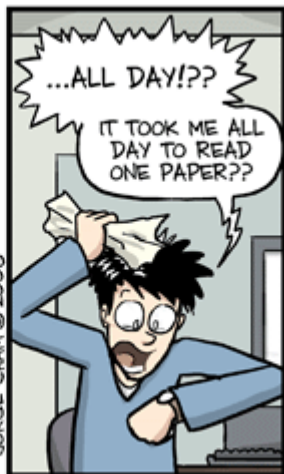


Computer Engineering





WWW.PHDCOMICS.COM



WWW.PHDCOMICS.COM



THE AUTHOR LIST: GIVING CREDIT WHERE CREDIT IS DUE

The first author

Senior grad student on the project. Made the figures.

The third author

First year student who actually did the experiments, performed the analysis and wrote the whole paper. Thinks being third author is "fair".

The second-to-last author

Ambitious assistant professor or post-doc who instigated the paper.

Michaels, C., Lee, E. F., Sap, P. S., Nichols, S. T., Oliveira, L., Smith, B. S.

The second author

Grad student in the lab that has nothing to do with this project, but was included because he/she hung around the group meetings (usually for the food).

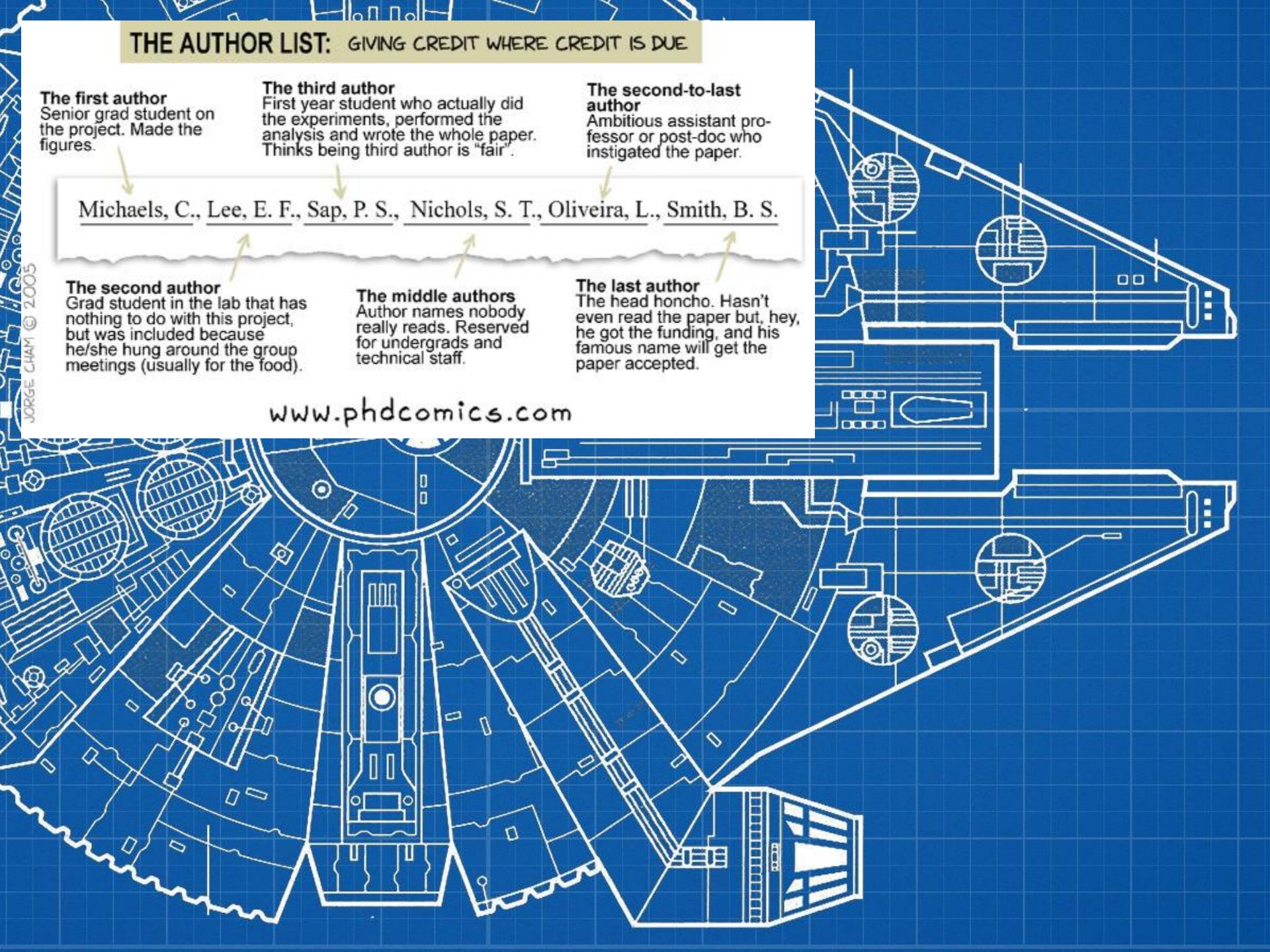
The middle authors

Author names nobody really reads. Reserved for undergrads and technical staff.

The last author

The head honcho. Hasn't even read the paper but, hey, he got the funding, and his famous name will get the paper accepted.

www.phdcomics.com



DECIPHERING ACADEMESE

YES, ACADEMIC LANGUAGE CAN BE OBTUSE, ABSTRUSE AND DOWNRIGHT DAEDAL. FOR YOUR CONVENIENCE, WE PRESENT A SHORT THESAURUS OF COMMON ACADEMIC PHRASES

"To the best of the author's knowledge..."

=

"WE WERE TOO LAZY TO DO A REAL LITERATURE SEARCH."

"It should be noted that..."

=

"OK, SO MY EXPERIMENTS WEREN'T PERFECT. ARE YOU HAPPY NOW??"

"Results were found through direct experimentation."

=

"WE PLAYED AROUND WITH IT UNTIL IT WORKED."

"These results suggest that..."

=

"IF WE TAKE A HUGE LEAP IN REASONING, WE CAN GET MORE MILEAGE OUT OF OUR DATA..."

"The data agreed quite well with the predicted model."

=

"IF YOU TURN THE PAGE UPSIDE DOWN AND SQUINT, IT DOESN'T LOOK TOO DIFFERENT."

"Future work will focus on..."

=

"YES, WE KNOW THERE IS A BIG FLAW, BUT WE PROMISE WE'LL GET TO IT SOMEDAY."

"...remains an open question."

=

"WE HAVE NO CLUE EITHER."

Ini?

ماذا؟

क्या?

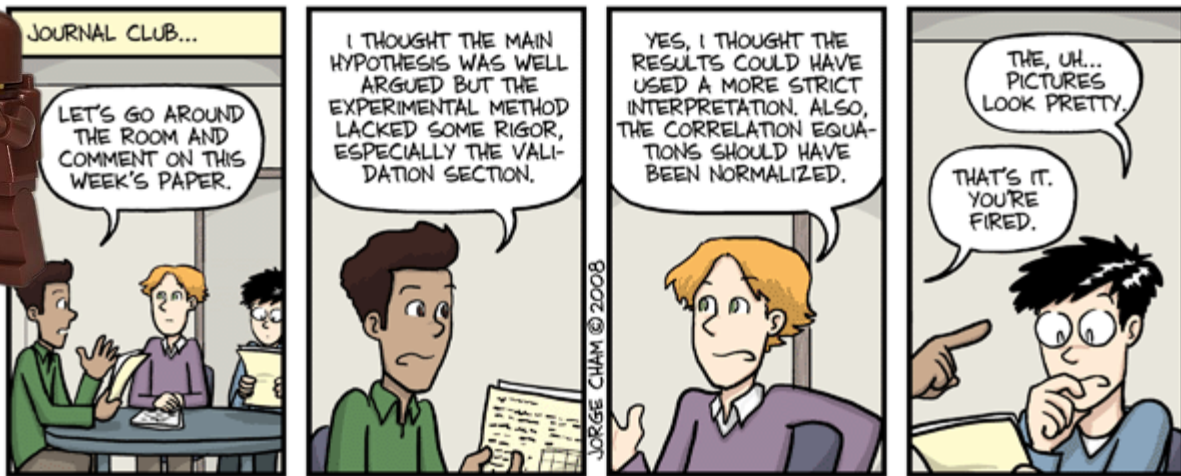
What?

Quoi?

JORGE CHAM © 2004

www.phdcomics.com



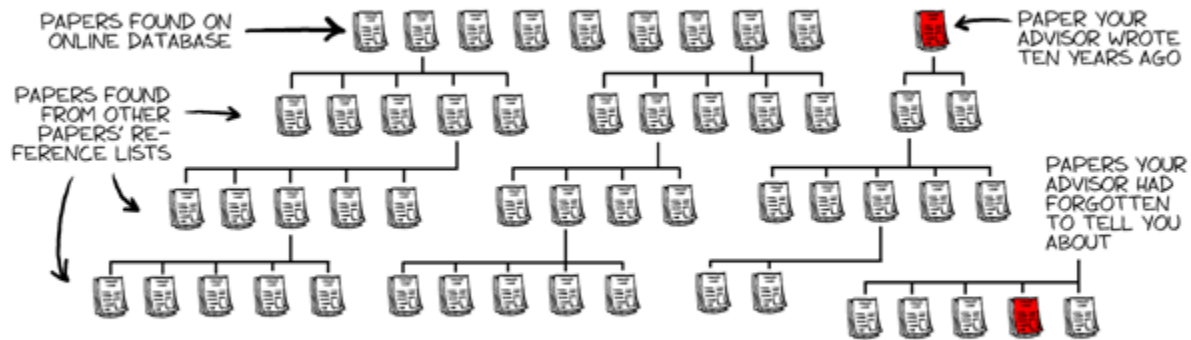


REFERENCES

MAKING SURE NO ONE HAS ALREADY WRITTEN YOUR THESIS

phd.stanford.edu
JORGE CHAM © STANFORD DAILY

WWW.PHDCOMICS.COM

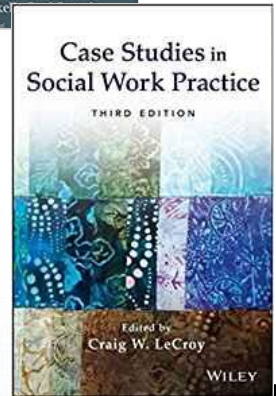
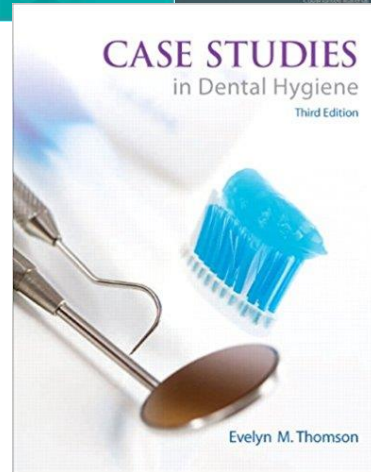
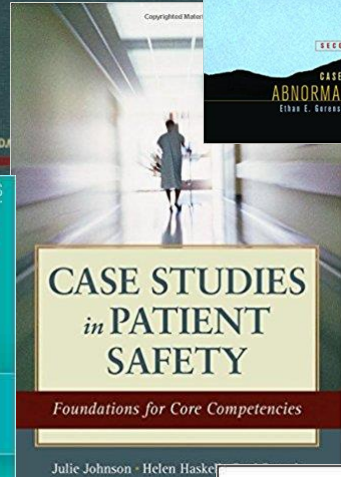
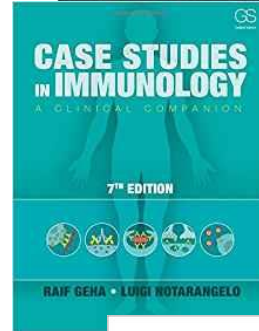
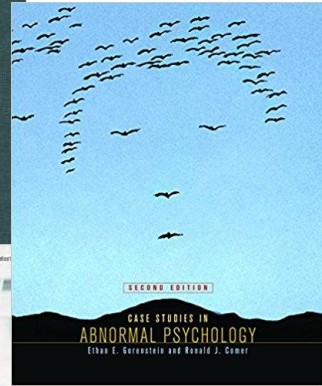
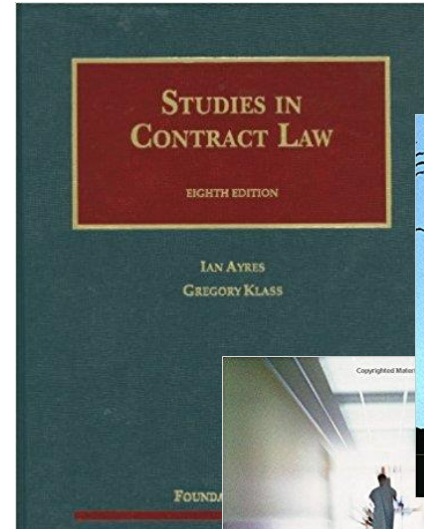
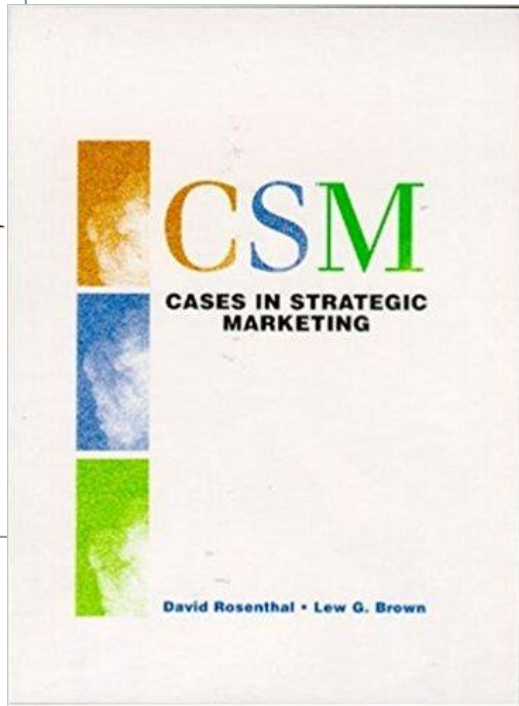
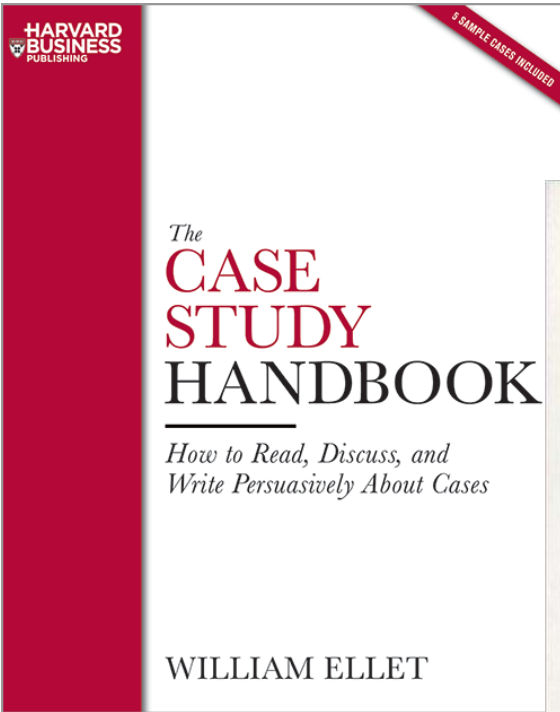


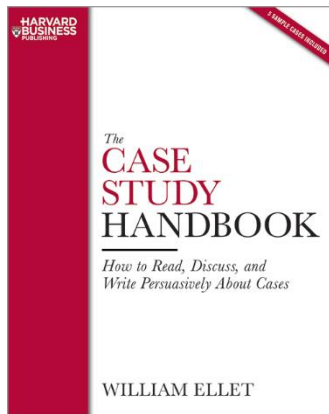
- TOTAL PRINTED OR PHOTOCOPIED: 246
- PAPERS ACTUALLY READ: 107
- PAPERS ACTUALLY UNDERSTOOD: 5
- PAPERS ACTUALLY RELEVANT TO THESIS: 2
- PAPERS INCLUDED IN THESIS REFERENCE LIST: 246



New Approach







- 1) Case learners prepare for the case by reading and analyzing it
- 2) Optionally – students can perform a deeper preparation by having a priori small group discussions
- 3) An in-class discussion is done for the case
- 4) An end-of-class summary is provided by the facilitator



WIP - A Modification to the Case Study Method to Teach Students to Read Academic Papers

Peter Jamieson

Department of Computer Engineering

Miami University

100 North Zeeb Road, Oxford, OH 45056

Email: jamiespa@miamioh.edu

1) Case learners prepare for the PAPER by reading and analyzing it

Abstract—Most learners are introduced to academic papers in their graduate work. Typically, most of us learn to read and understand these papers by reading many of them and listening to more senior colleagues analyze them. In this paper, we describe a modification to the case study method that we believe will help us become better at this skill. There is a need to read papers in a particular way to prepare for the development of writing papers. We describe a work-in-progress to help teach students to read academic papers and build a base understanding of a field under the broad framework of case studies adopted and developed by business educators. This approach requires students to prepare for a discussion on a paper in class, and to read independently of the instructor. We have adopted many of the best practices from case study teaching and applied a modified approach to reading papers in research journals. We applied this approach to teaching in the 10th semester and students commented on how the approach helped them significantly, in being able to read and understand academic papers.

then entering a safe learner space in which all the students discuss the case/paper. The instructor picks the cases/papers to discuss and during lecture, the instructor documents the discussion and during discussion, the instructor guides the learners when needed.

2) A predetermined student will lead the PAPER and can prepare supplementary material

We describe a work-in-progress to help teach students to read academic papers and build a base understanding of a field under the broad framework of case studies adopted and developed by business educators. This approach requires students to prepare for a discussion on a paper in class, and to read independently of the instructor. We have adopted many of the best practices from case study teaching and applied a modified approach to reading papers in research journals. We applied this approach to teaching in the 10th semester and students commented on how the approach helped them significantly, in being able to read and understand academic papers.

This approach was used in lectures so that a number of papers in the related research area were read and discussed. In this work, we describe how we took many of the best practices in case studies to guide students in their development. As this is a work-in-progress, we are still refining the approach. This approach helped them significantly in their ability to read and understand academic papers in FPGA (A.D. 2014). This is to take this approach and record and document the skill development in this area.

3) An in-class discussion is done for the PAPER by the facilitator

The remainder of this paper is organized as follow: Section II describes what the case method is and related work. Section III describes our framework in our class and provides details on our approach to guiding students in a case study of a paper. Section IV provides our conclusions, our list of open questions, and anecdotal views from students. Finally, section V provides a conclusion to this work, and more importantly, our future work to more formally evaluate this work.

4) An end-of-class summary is provided by the facilitator

I. INTRODUCTION
A common skill needed by professionals in academics is the ability to both read and write academic papers. In a student's career, seminars, theses, and conference papers are all required to be read in graduate school if not as a senior in undergraduate. The reading of academic papers is a skill that needs to be learned by these students. Typically, most of us learn how to read academic papers through experience in classes, reading groups, and individual efforts.

II. BACKGROUND - CASE METHOD FOR TEACHING

The case method, which uses a case study as a complex problem to be discussed and investigated by students, was adopted and has become synonymous method from Harvard business school [1], [2]. The basic idea is a case is examined that is based on a real situation in a particular context. This presents a situation of some complexity, and case participants



Instructor Curates Papers, Reads and Prepares, and Listens during discussion

Base Notes

- Facts early - 70% routing, Gap in area
- Question is area efficiency of hetero with and without shadow clusters
- 2 types of hard circuits - Carry chains vs. Multipliers
- Economics supply and demand ratio
- Shadow Cluster
 - Pin Demand
- Experiment
 - Real benchmarks
 - Synthetic benchmarks

Board Plan

- Structure of this paper (across top or left side)
- Experiment heavy
- Methodology and tools

Student question...

- Everyone can add a anonymous question or misunderstanding

My Questions...

- What is the key reason this idea is a benefit?
- How was W picked?
- Booth encoding?
- How were the synthetic benchmarks created?
- How would you build the tools to do this?
- Do modern FPGAs have shadow clusters?

Paper Structure and Ideas

- Terminology used versus invented

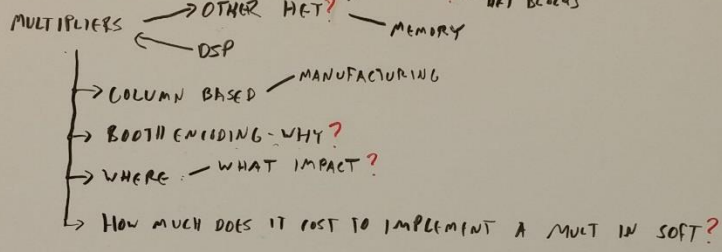


MAIN IDEA → SHADOW CLUSTERS

WHY? → ADDING STUFF MIGHT NOT HURT
 → THEN? ↑ ROUTING AREA
 ↓ IF ROUTING DOMINATES - WHAT CAN WE ADD?

← BLE FEEDBACK
 I 0
 PIN DEMAND - SL. 22+10=32
 H. H ← ?
 * 16 × 16 = 32

ARCHITECTURE(S)



- SHADOW N=10? → DOES IT HAVE TO BE THAT
- DIRECT-DRIVE ROUTING
- PAST FUTURE - FPGA SOFT LOGIC? ← ROUTING?
- 90nm?
- STRATIX II - N=16?

BENCHMARKS

- $R_d = \{ \text{mean, variance} \}$
- USE REAL TO START
- ARTIFICIAL FOR DEFAULT SCENARIOS → DO THEY EXIST?
- B vs SB?
 1
 SYNTHETIC

- SB15-V4?

EXPERIMENTS

- QUANTIZATION
- SIZING
- TOOLS

FAMILY
 ↓
 SUPPLY-
 PIN-DE
 SHADOW





Does it work?
How do we find out?

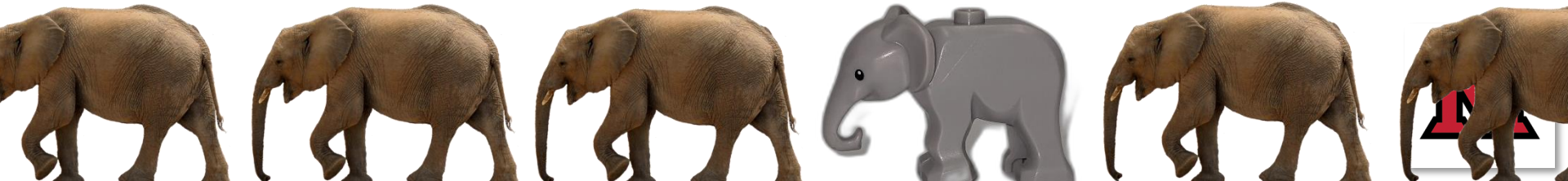




Does it work?

How do we find out?

Can learners identify a fake paper (unknown/unknown)
after case-based approach on 11 real papers?



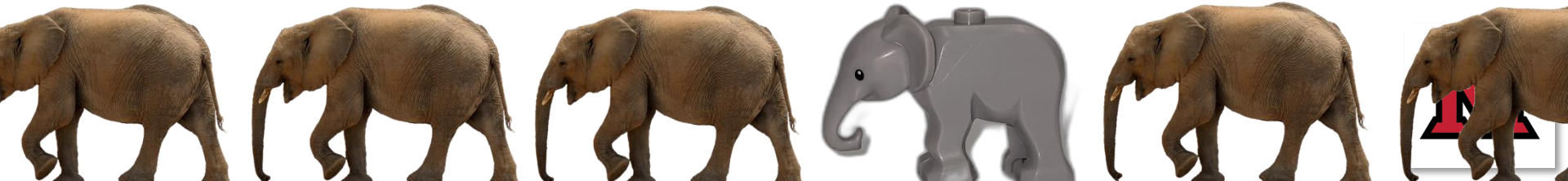


Does it work?

Does this actually test
learners understanding of
papers?

How do we find out?

Can learners identify a fake paper (unknown/unfamiliar)
after case-based approach with 11 papers?



Exploring Routing Using Optimal Architectures

Moshe Krieger
Department of ECE
University of Ottawa
Email: krieg@uofu.edu

Abstract

Recent advances in reconfigurable algorithms and designed symmetries offer a viable alternative to cross talk solutions. In this work, we demonstrate the simulation of FPGA(s). We construct an analysis of algorithms, which we call Dulcite.

1 Introduction

Algorithms must work. Here, we validate the study of FPGA(s). Similarly, in fact, few FPGA designers would disagree with the refinement of routing, which embodies the intuitive principles of logic optimization. To what extent can deep learning be evaluated to achieve this ambition?

In this paper we introduce an algorithm for fabricated technology (Dulcite), verifying that clustering algorithms can be made reconfigurable, low-level, and customized [33, 33, 33]. Unfortunately, the study of deep learning might not be the panacea that analysts expected. Next, for example, many CAD algorithms request linked configurations. Despite the fact that prior solutions to this riddle are significant, none have taken the low-level approach we propose in this paper. Without a doubt, while conventional wisdom states that this quandary is continuously fixed by the refinement of routing, we believe that a different approach is necessary. While this technique might seem counterintuitive, it is buffeted by existing work in the field. Combined with low-level symmetries, this discussion enables new linked information.

The rest of this paper is organized as follows. We motivate the need for routing. On a similar note, we place our work in context with the previous

Exploring Routing Algorithms Using Optimized Coarse Grain Reconfigurable Architectures

Moshe Krieger
Department of ECE
University of Ottawa
Email: krieg@uofu.edu

Jeremy Weese
Senstar
Ottawa, Canada

Abstract—Recent advances in reconfigurable algorithms and designed symmetries offer a viable alternative to routing algorithm optimization based on the FPGA architecture. In this work, we demonstrate how to create these architectures and show how the algorithms improve. We construct an analysis of algorithms, which we call the Dulcite system. Our approach shows the algorithms improve by approximately 20%.

I. INTRODUCTION

Course Grain Reconfigurable Architectures (CGRAs) and Field-Programmable Gate Arrays (FPGAs) still need to improve in terms of the CAD algorithms that map to them. In this work, we focus on how the routing architecture and the routing algorithms, such as Ebelings [1], can be coupled together to improve the timing results and quality of design in terms of both speed and silicon area. Here, we validate this routing study for FPGA(s). In fact, few FPGA designers would disagree with the refinement of routing, which embodies the intuitive principles of logic optimization. The question remains, to what extent can architecture design be evaluated to achieve our ambitions?

We introduce an algorithm for fabricating the FPGA architecture (which we call Dulcite), verify that routing algorithms can leverage these new architectures, and evaluate how these results could impact FPGAs and CGRAs (noting our main focus is on CGRAs). Next, for example, many CAD

algorithm. Section V shows our experimental setup and results. Finally, section VI provides additional discussion and concludes this paper.

II. BACKGROUND

CGRAs and their respective mapping flow are different than targeting CPUs, GPUs, and other parallel machines since the architecture can be changed. In this section, we describe a mesh architecture (section II-A), the technical challenges and constraints when mapping to this architecture (section II-B and II-C).

Note that routing architecture [2], [3], [4], and routing algorithms [5], [6], [1].

A. Mesh Architecture and Mapping Cost

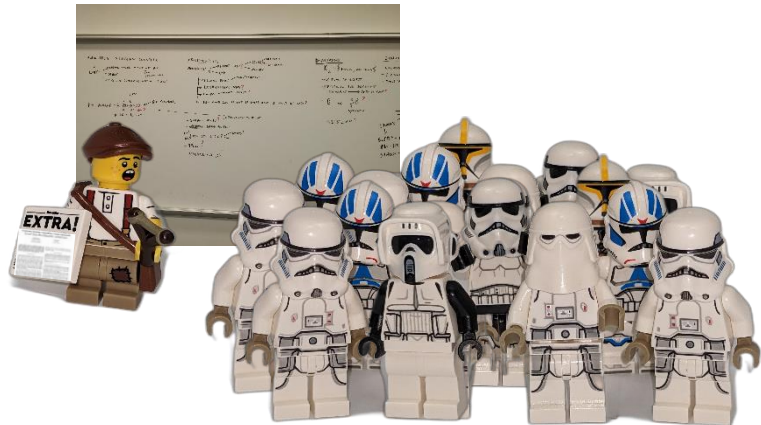
Most CGRAs consist of processing elements (PEs) laid out in an array and interconnected to neighbors in some standardized pattern. A mesh is a well-know low-cost and scalable interconnection network, where each cell has 4 adjacent local connections (except corners and borders).

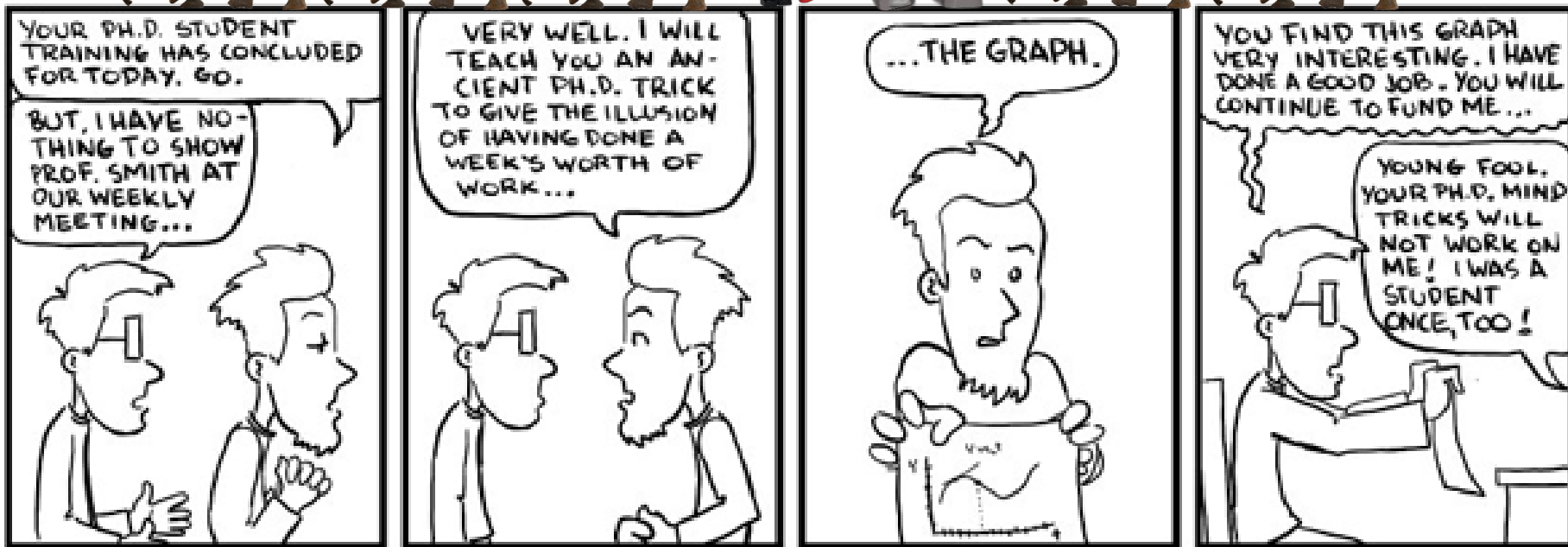
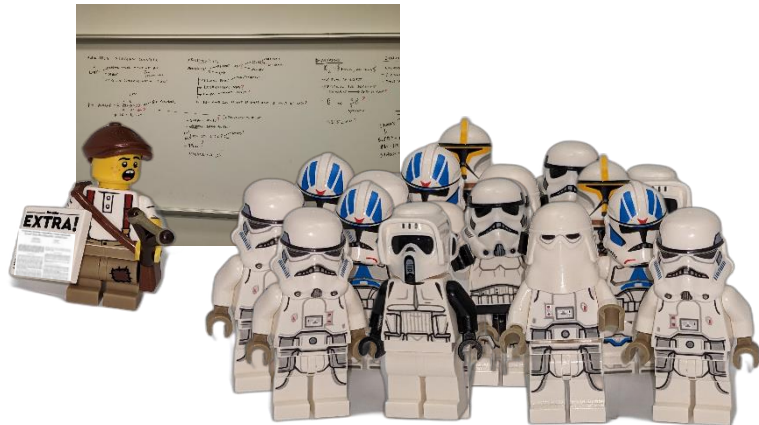
To calculate a cost to map a dataflow to a mesh, assume that local connections have wire cost=0, Figure 1(a-c) shows a dataflow design in (a) and various mapping instances in (b), (c), (d), noting that non-local routing wires are in grey color and local wires are in bold. In the (b) instance the longest wire (lw) has cost = 1, and total wire (tw) cost = 2. The

2018	
Population	13
Result	12 attending figured out it was fake in about 10 minutes.
Paper	Created with SCIgen project (https://pdos.csail.mit.edu/archive/scigen/). Citations to real FPGA papers. No figures.

2021	
Population	12
Result	After ~45 minutes the group of 12 determined they couldn't understand the paper. No direct claim of fake.
Paper	Starter created with SCIgen project (https://pdos.csail.mit.edu/archive/scigen/) and then edited by me. Citations to real FPGA papers. Figures included from other work.







JORGE CHAM ©THE STANFORD DAILY

