Improving the Area-Efficiency of FPGAs with Shadow Clusters

Peter Jamieson and Jonathan Rose

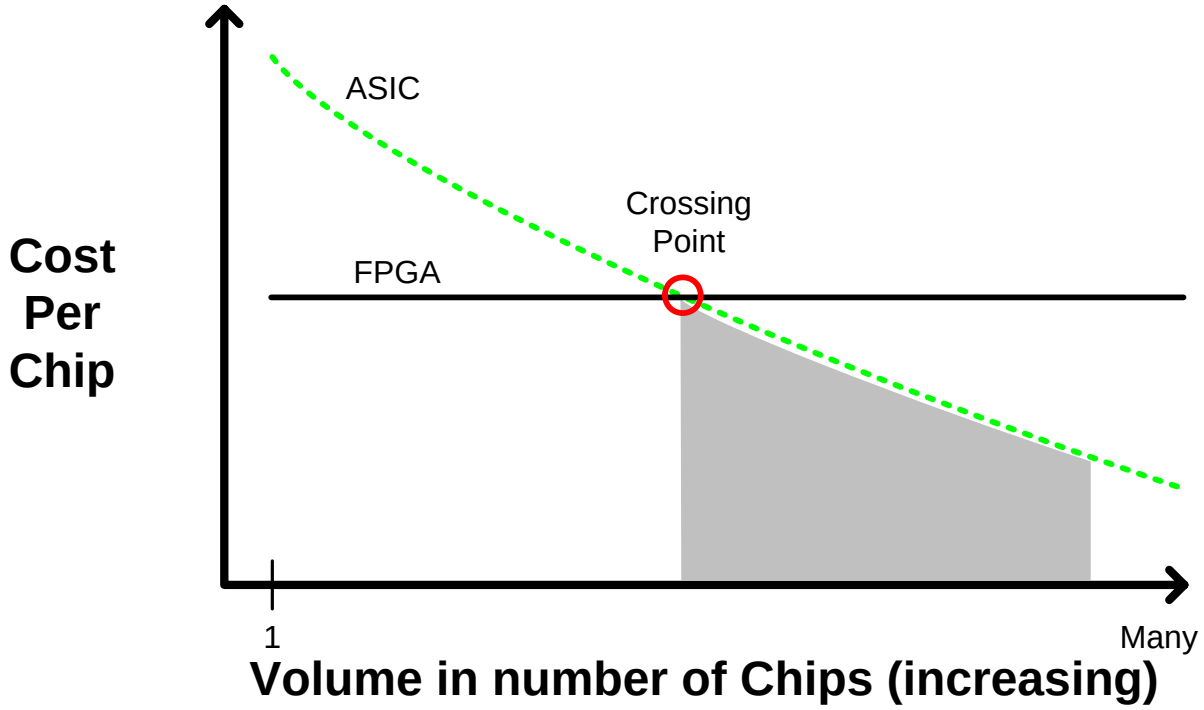
University of Toronto

Why Do We Care About Area-Efficiency?

- Didn't we finish worrying about that a while ago?
- Recall:
  - FPGA conquer ASIC
  - The GAP between FPGAs & ASICS

    35x area, 4x speed, 10x power

Making FPGAs Better – Area = Cost



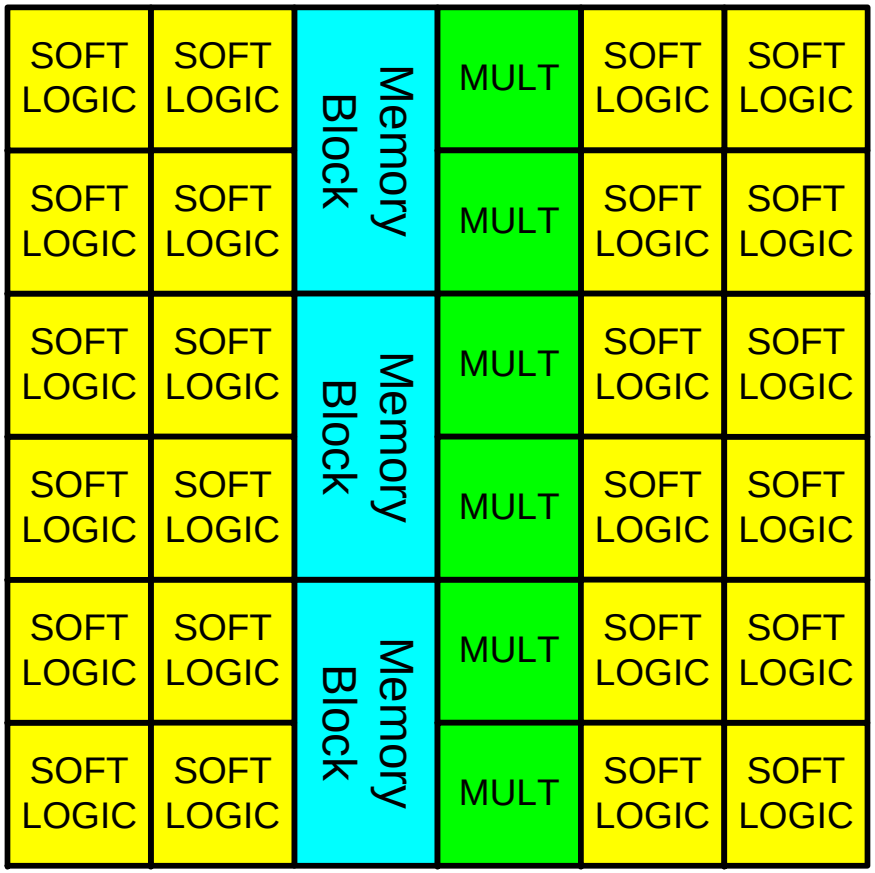
Improved FPGA area-efficiency - sell more chips!

One Way to Improve Area-Efficiency

USE Dedicated hard circuits:

- e.g. multiplier tile
- e.g memory block tile

– 22x Area Gap



Hard Circuits

- Why not add more hard circuits?

  "Should add circuit **X** to FPGA since it would be useful to me!"

  – Quote from Novice Architect

- Need a scientific way to make the decision of what to include as a hard circuit

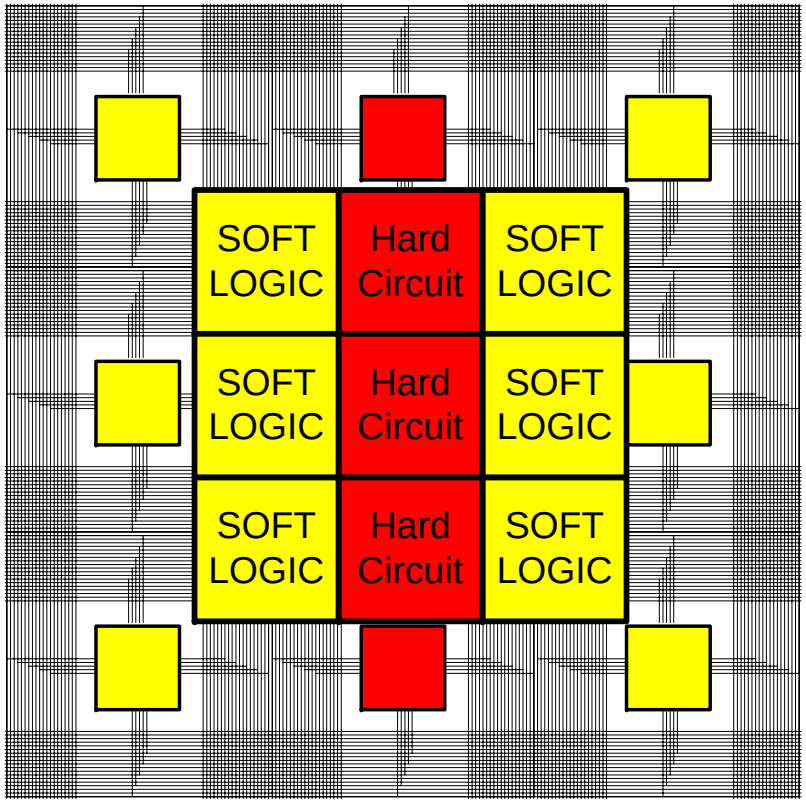
Conditions to Add a Hard Circuit

1. Hard circuit provides a benefit
   - Area, Speed, Power consumption, or mix

2. Significant portion of FPGA Market uses that hard circuit

Hard Circuit: Good or Bad

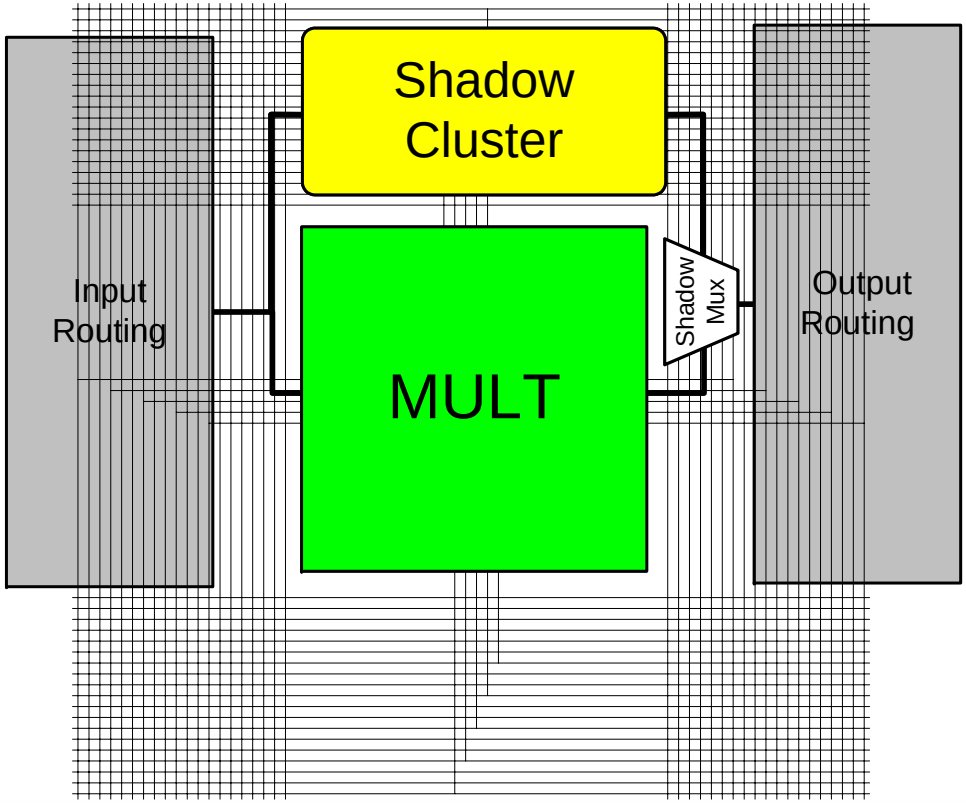
- Hard circuits provide benefit *when used*
  - Wasted Area for Hard Circuit
  - Routing resources wasted!!!
  - 70-90% of FPGA area occupied by routing



Shadow Clusters: New Idea

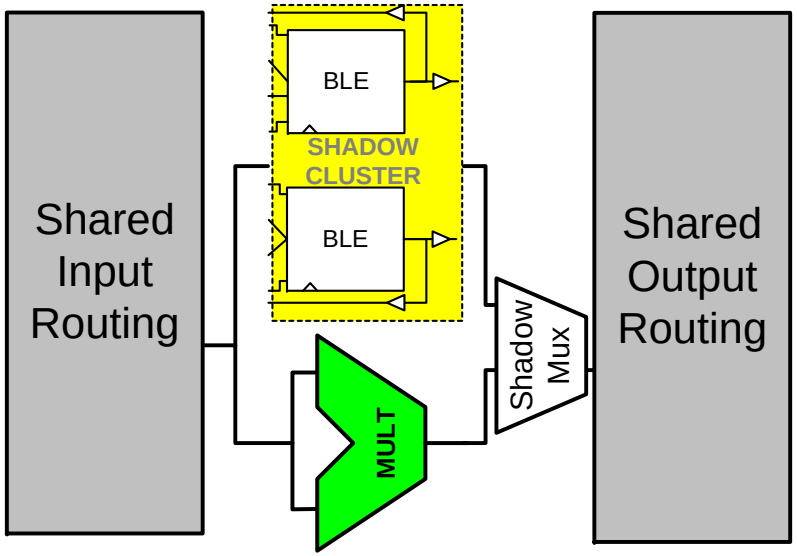
- Combine with soft logic

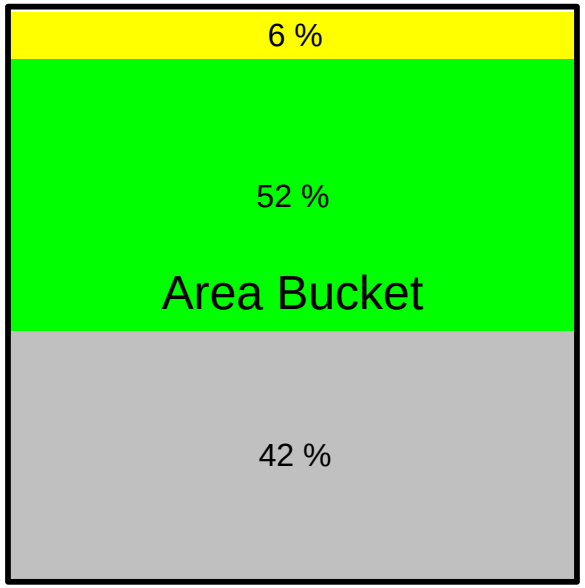
SHADOW CLUSTER



The Gain

- Tile always used – no wasted routing
- In the multiplier case…
  - 42% area for Routing!!!





Today

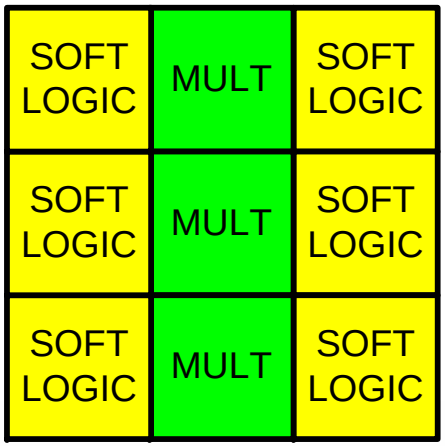
- Scientific method to measure area-efficiency of hard circuits
- Measure area-efficiency improvement of architecture with shadow cluster

How many hard circuits?

- FPGA Architecture's Supply Ratio: R_S

 # hard circuit tiles : # soft logic cluster tiles

Example: R_s = 1:2



Industrial Multiplier Supply Ratios

FPGA	Stratix I	Stratix II	Virtex II	Virtex 4 (SX)	Virtex 4 (FX)	Virtex 4 (LX)
Supply Ratio	1:66	1:45	1:23	1:15	1:60	1:104

- Normalized to 18x18 multipliers
- Increasingly large multipliers need 10 LUT cluster
- Sub-families try to match supply to markets
  - Virtex4 and 5
  - StratixIII

Circuits Demand

- User Circuit's Demand Ratio: R_D

 # hard circuit tiles : # soft logic cluster tiles

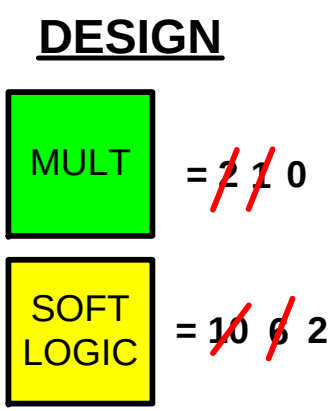
  - Assumes all hard circuits in the circuit can map to hard circuit on FPGA

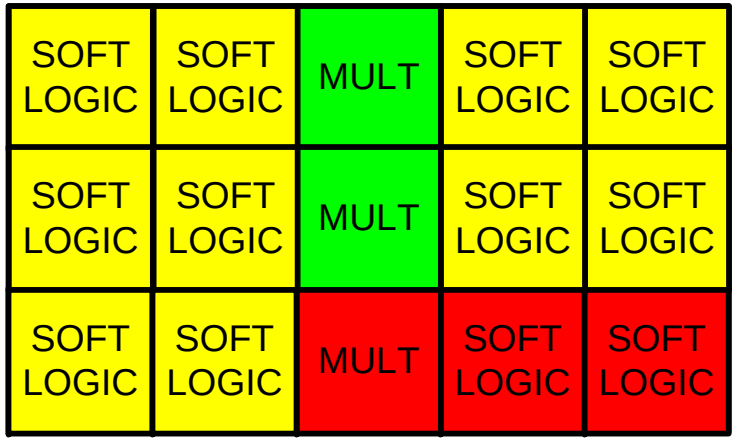
Is there always a benefit with Shadow Clusters?

- Depends on relation between supply and demand
  - 2 Cases

Mapping Design to an FPGA

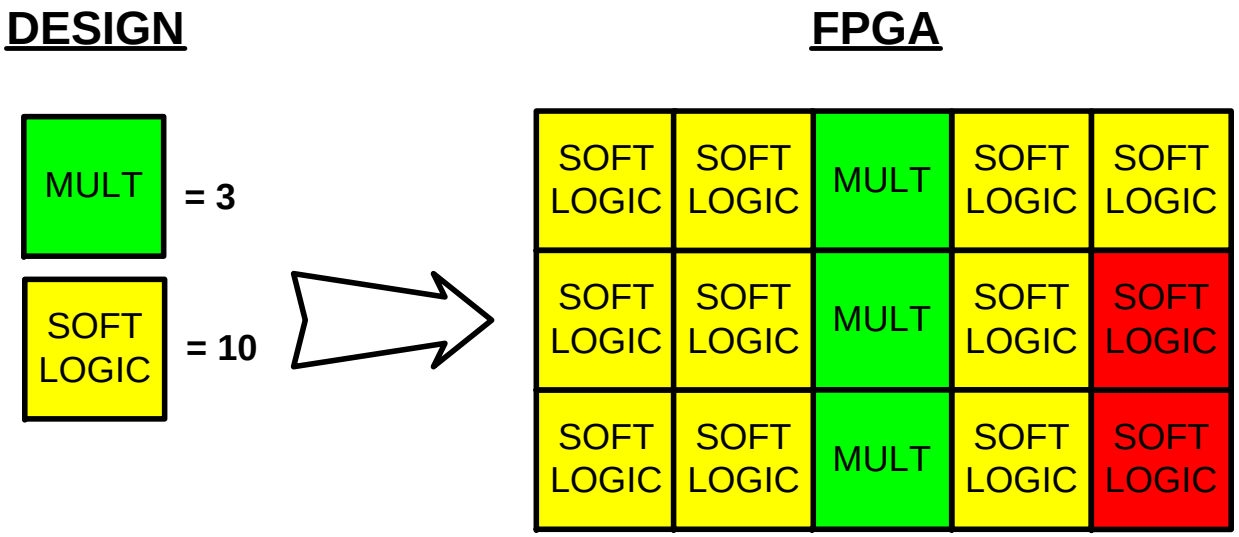
- Step by Step mapping
  - Design
    - R_D = 1:5
  - FPGA
    - R_S = 1:4





Case 1 – Demand >= Supply

- Supply Ratio: 1 mult. for every 4 soft logic clusters



☞Every tile employed for primary purpose

☞Shadow Concept Loses!

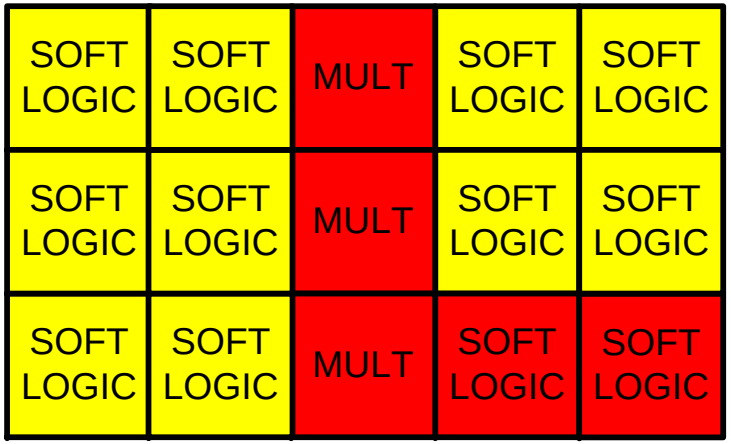
Case 2 – Demand < Supply

DESIGN

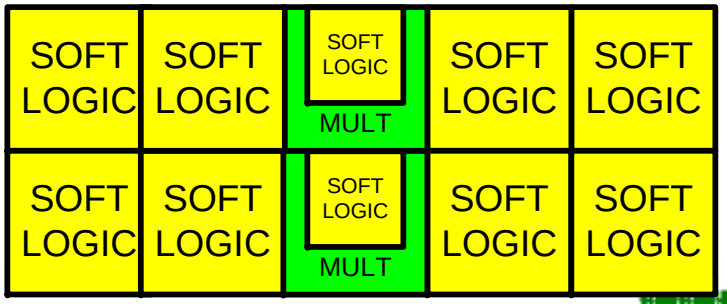
MULT = 0

SOFT LOGIC = 10

FPGA - without Shadow Clusters



FPGA - with Shadow Clusters



Here, shadow cluster FPGA wins!!!

Question

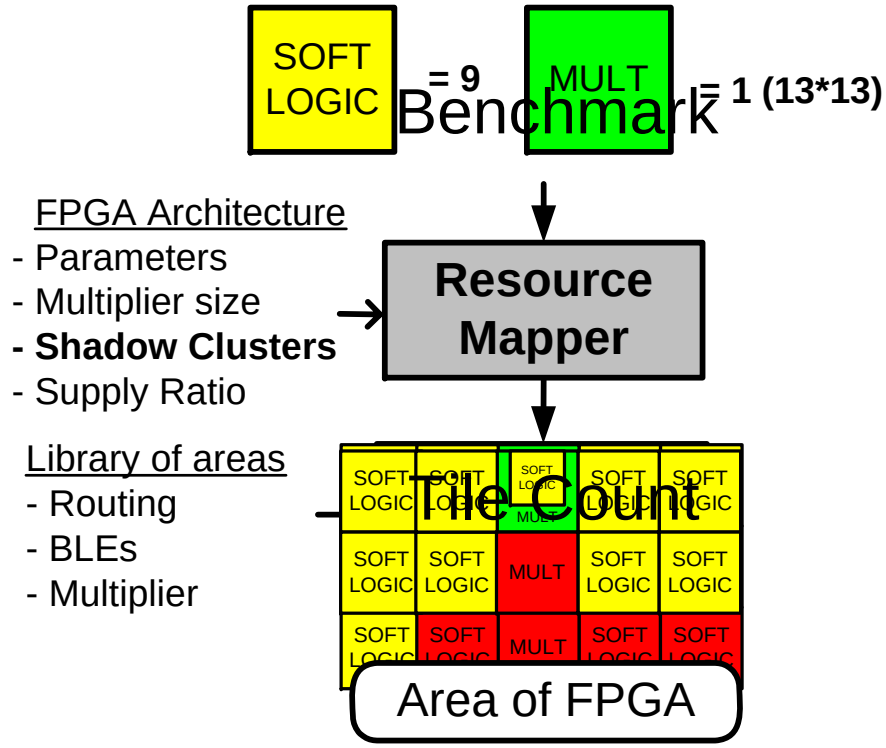
- Depending on how often Case 1 and 2 happens, will win or lose.

How much do shadow clusters improve area-efficiency of FPGAs?

Measurement Methodology

Empirical

1. Map Benchmarks to tiles on FPGA
2. Calculate Area



Tile Area

- Key to our measurement
- Soft Logic Cluster Tile
  - Our own tool
- Multiplier
  - Mapped to standard cells

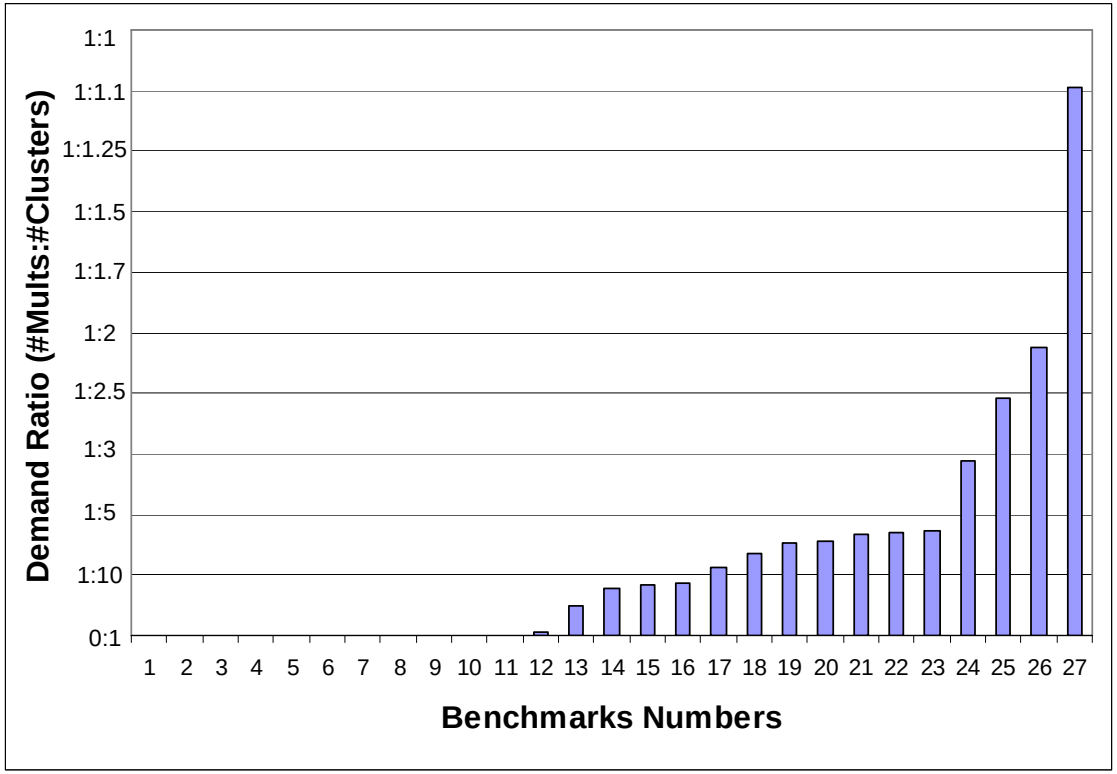
Relative Tile Area - Multipliers

Tile Type	BLEs	Multiplier	Routing	Relative size / tile
Cluster	13%	-	87%	1.0
Multiplier 18x18	-	55%	45%	3.8
Multiplier 18x18 + Shadow Cluster	6%	52%	42%	4.0

Benchmarks

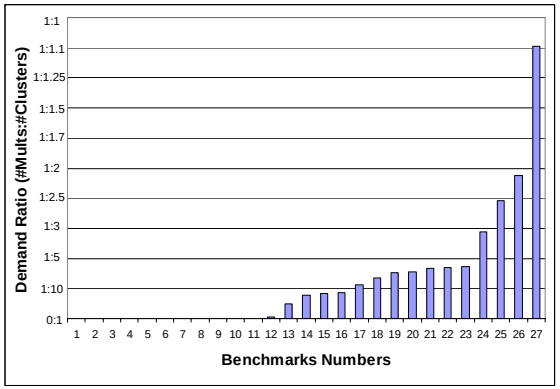
- 27 existing benchmarks
  - Avg. Demand Ratio = 1:8
- For statistical study we use synthetic benchmarks

Benchmarks Demand Ratio Distribution



Avg. Demand = 1:8 – Very high

Synthetic Benchmarks – Real Distribution



Name	Num Bmarks.	Avg Demand	BLE Range	Mult. Range
B8	27	1:8	10542 to 34379	0 to 528
SB45	250	1:45	10000 to 25000	0 to 145
SB15_V2	250	1:15	10000 to 25000	0 to 350

Experiments: Area-Efficiency Ratio

- Each benchmark area ratio

$$\frac{\text{Area}_{\text{FPGA with mults}}}{\text{Area}_{\text{FPGA with mults+shadow}}}$$

  - **“>1”** means Shadow Cluster Architecture smaller

- Geometrically average area ratios
  - For each benchmark in suite

Experiment 1: Shadow vs Non-Shadow Architectures

- Shows how shadow clusters affect each benchmark
  - SB15
    - 10 benchmarks

Results

# Soft Logic Clusters	#Multipliers (18x18)	Demand Ratio	Area		Area-Efficiency Ratio
			No Shadow Clusters	Shadow Clusters	
1849	0	0	170	152	**1.118**
1638	0	0	151	135	**1.086**
1420	0	0	131	117	**1.119**
1042	0	0	96	87	**1.110**
1904	0	0	174	156	**1.115**
1924	89	1:21.6	175	171	**1.023**
1523	141	1:10.8	204	207	**0.986**
1309	121	1:10.8	175	177	**0.986**
1528	284	1:5.4	411	417	**0.986**
1502	349	1:4.3	506	513	**0.986**
		Average: 1:15			Average: **1.054**

Experiment 2: Best Shadow and Non-Shadow Architecture

- Allow the supply ratio to vary
- Map benchmark suites to
  - Shadow
  - Non-Shadow

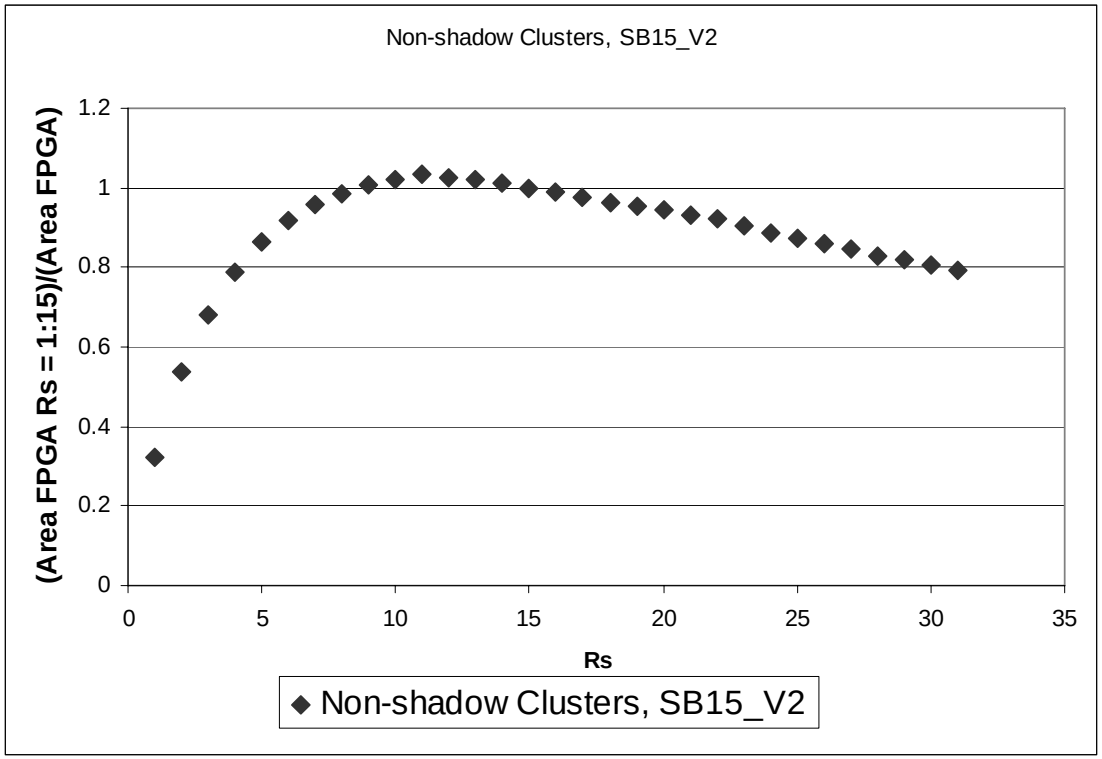
Best Shadow and Non-Shadow Architecture – Part 1

- Compare both shadow and non-shadow
  - base_non_15 = non-shadow, supply = 1:15

- Area ratio per benchmark

$$\frac{\text{Area}_{\text{base\_non\_15}}}{\text{Area}_{\text{experimental architecture}}}$$

Best Non-Shadow Architecture

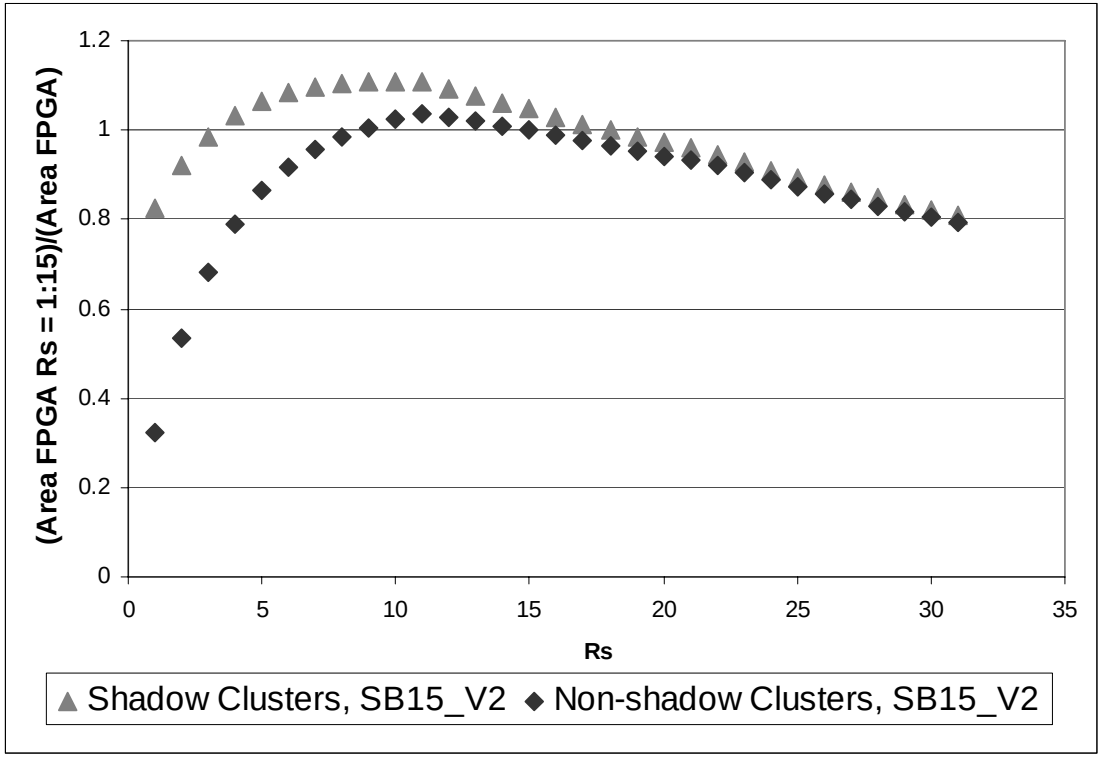


Best Non-Shadow Architecture Supply = 1:13

Best Shadow Architecture

Best Shadow Architecture Supply = 1:11

Best Shadow and Non-Shadow Architecture – Part 1



Best Shadow and Non-Shadow Architecture – Part 2

- Lets look at a few benchmarks suites

Benchmark Name	Non-shadow supply ratio	Shadow supply ratio	Non Shadow vs Shadow area
B8	1:11	1:9	12.5%
SB15_V2	1:13	1:11	7.2%
SB45	1:28	1:19	4.6%

General Conclusions

- Shadow Cluster improve area-efficiency of FPGAs
  - Existing hard circuits (multiplier)
- 12.5% Improvement with Shadow Clusters
- Never lose

Future Work

- Crossbar work
  - Can we add them now?
- Multiple hard circuits